



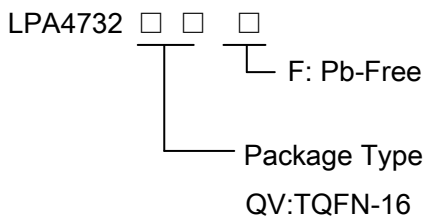
## 215mW TrueCapFree Stereo Headphone Amplifier

### General Description

The LPA4732 stereo headphone amplifiers are designed for portable equipment where board space is at a premium. The LPA4732 deliver up to 215mW per channel into a 16Ω load or 194mW into a 32Ω load and have low 0.006% THD+N. An 78dB at 217Hz power-supply rejection ratio (PSRR) allows these devices to operate from noisy digital supplies without an additional linear regulator. Comprehensive anticlick-and-pop circuitry suppresses audible clicks and pops on startup and shutdown. A low-power shutdown mode reduces the supply current to 0.1μA.

The LPA4732 operates from a single 2.5V to 5.5V supply, consumes only 5mA supply current, and is specified over the extended -40 °C to +85 °C temperature range. The devices are available in tiny 16-pin TQFN (3mm× 3mm×0.8mm) packages.

### Order Information



### Applications

- ✧ MP3 Players
- ✧ Smart/Cellular Phones
- ✧ PDAs
- ✧ Portable Audio
- ✧ Notebook and Desktop PCs
- ✧ Flat-Panel Monitors

### Features

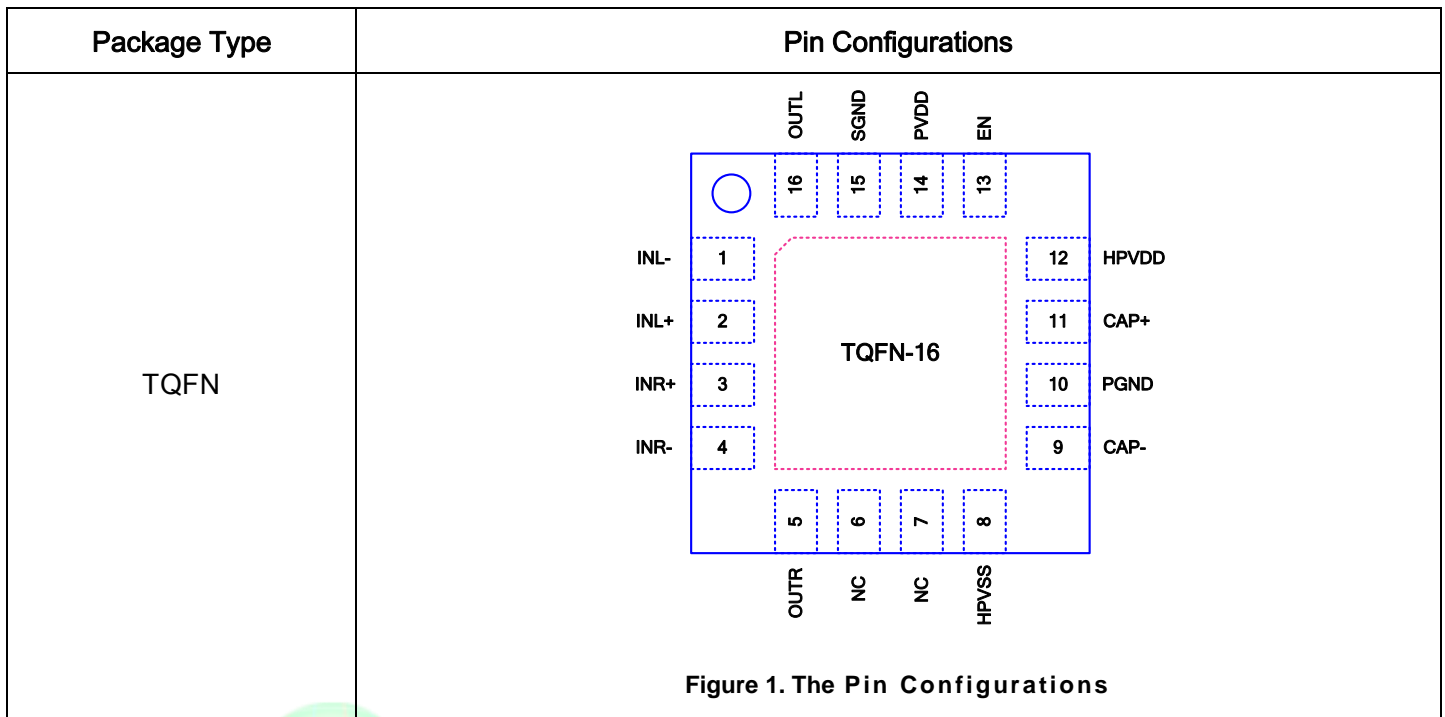
- ◆ 2.5V to 5.5V Single-Supply Operation
- ◆ No Bulky DC-Blocking Capacitors Required
- ◆ No Degradation of Low-Frequency Response Due to Output Capacitors
- ◆ Differential Inputs for Enhanced Noise Cancellation
- ◆ 215mW into 16Ω Load from 5V Power Supply at THD+N = 1% (TYP, per Channel)
- ◆ Low 0.006% THD+N
- ◆ High PSRR (-80dB at 217Hz)
- ◆ Short-Circuit and Thermal-Overload Protection
- ◆ Integrated Click-and-Pop Suppression
- ◆ Low Quiescent Current (3mA at VDD = 5V)
- ◆ Enable Control
- ◆ Under-Voltage Lockout Function
- ◆ -40°C to +85°C Operating Temperature Range
- ◆ Available in a Space-Saving 16-Pin TQFN (3mm× 3mm× 0.8mm) Package

### Marking Information

Device	Marking	Package	Shipping
LPA4732QVF	LPS LPA4732 YWX	TQFN-16	3K/REEL
Y: Y is year code. W: W is week code. X: X is series number.			



## Functional Pin Description



## Pin Description

PIN	NAME	DESCRIPTION
1	INL-	Inverting left input for differential signals.
2	INL+	Non-inverting left input for differential signals.
3	INR+	Inverting right input for differential signals.
4	INR-	Non-inverting right input for differential signals.
5	OUTR	Right headphone amplifier output. Connect to right terminal of headphone jack.
6,7	NC	No connection.
8	HPVSS	Charge pump output and negative power supply for output amplifiers; connect 1uF capacitor to GND.
9	CAP-	Charge pump negative flying cap.
10	PGND	Power Ground.
11	CAP+	Charge pump positive flying cap.
12	HPVDD	Positive power supply for headphone amplifiers. Charge pump positive half VDD output.
13	EN	Amplifier enable. Connect to logic low to shutdown; connect to logic high to activate.
14	PVDD	Power VDD.
15	SGND	Amplifier reference voltage.
16	OUTL	Left headphone amplifier output. Connect to left terminal of headphone jack.
-	EP	Exposed Paddle. Electrically connect to PGND or leave unconnected.



### Typical Application Circuit

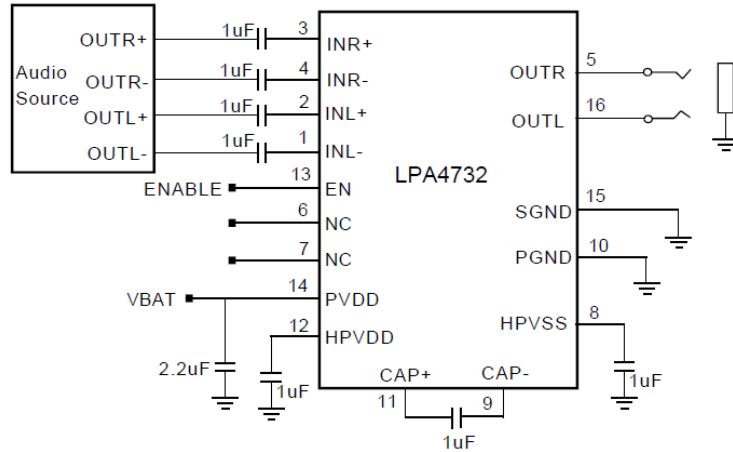


Figure 2. Typical Differential Input Application Circuit

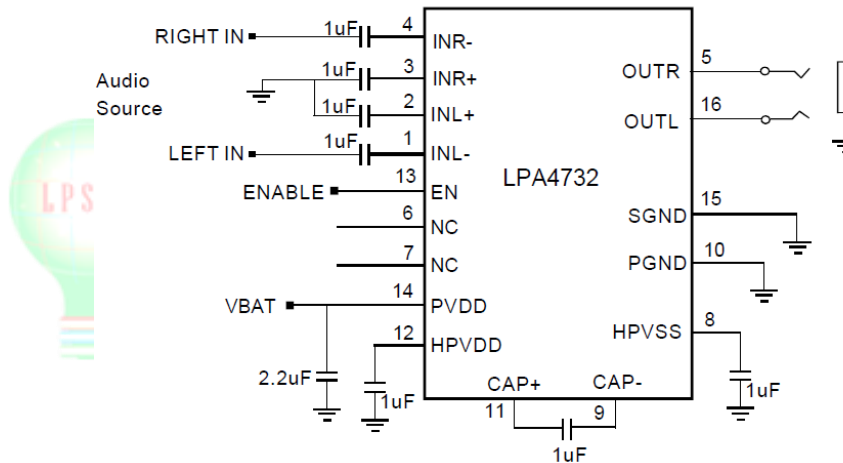


Figure 3. Typical Single-Ended Input Application Circuit

### Absolute Maximum Ratings

These are stress ratings only and functional operation is not implied. Exposure to absolute maximum ratings for prolonged time periods may affect device reliability. All voltages are with respect to ground.

Supply Voltage (PVDD) .....	6.0V
Input Voltage (INR+, INR-, INL+, INL-).....	HPVSS-0.3V to HPVDD+0.3V
Control Interface Voltage.....	-0.3V to PVDD+0.3V
Junction Temperature .....	+150°C
Storage Temperature Range .....	-65°C to +150°C
Lead Temperature (Soldering, 10s) .....	+260°C

### Thermal Information

Thermal Resistance (TQFN-16, JA) ----- 48°C/W



## ESD Susceptibility

HBM (Output pins to Supply and Ground pins) ..... 2000V

## Recommended Operating Conditions

Supply Voltage Range ..... 2.5V to 5.5V

Operating Temperature Range ..... -40°C to +85°C

## Electrical Characteristics

TA=25°C, PVDD=3.6V, RL=16Ω (unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Units
<b>GENERAL</b>						
Quiescent Supply Current	I <sub>Q</sub>	EN=PVDD, No load		3		mA
Shutdown Supply Current	I <sub>SD</sub>	EN=0V, PVDD=2.5V to 5.5V		0.1	1	μA
EN Input Logic High	V <sub>IH</sub>		1			V
EN Input Logic Low	V <sub>IL</sub>				0.6	V
EN to Full Operation Time	t <sub>SON</sub>			1.6		ms
<b>AMPLIFIERS</b>						
Output Offset Voltage	V <sub>OS</sub>	Between OUTL(OUTR) and GND, input AC-coupled to ground.		0.2	2	mV
Common Mode Rejection Ratio	CMRR	Input referred, LPA4732, T <sub>A</sub> = +25°C	-70	-86		dB
Power Supply Rejection Ratio	PSRR	f = 217Hz, 100mV <sub>P-P</sub> ripple, input referred		-80		dB
		f = 10kHz, 100mV <sub>P-P</sub> ripple, input referred		-60		
Output Power	P <sub>OUT</sub>	PVDD=5V, RL = 16Ω, THD+N = 1%		215		mW
		PVDD=5V, RL = 32Ω, THD+N = 1%		194		
		PVDD=3.6V, RL = 16Ω, THD+N = 1%		115		
		PVDD=3.6V, RL = 32Ω, THD+N = 1%		105		
Total Harmonic Distortion Plus Noise	THD+N	RL = 16Ω, P <sub>OUT</sub> = 55mW, f = 1kHz		0.008		%
		RL = 32Ω, P <sub>OUT</sub> = 125mW, f = 1kHz		0.007		
Signal-to-Noise Ratio	SNR	RL = 32Ω, P <sub>OUT</sub> = 20mW, f = 22Hz to 22kHz		100		dB
Noise	V <sub>n</sub>	22Hz to 22kHz bandwidth, input AC		7		μV <sub>RMS</sub>
Capacitive Drive	C <sub>L</sub>	No sustained oscillation	47	200		pF
Charge-Pump Oscillator	f <sub>OSC</sub>			500		kHz
Crosstalk		RL = 32Ω, V <sub>IN</sub> = 200mV <sub>P-P</sub> , f = 10kHz, A <sub>V</sub> = 1		80		dB
Thermal Shutdown Threshold				145		°C
Thermal Shutdown Hysteresis				5		°C

**Note 1:** All specifications are 100% tested at TA = +25°C; temperature limits are guaranteed by design.

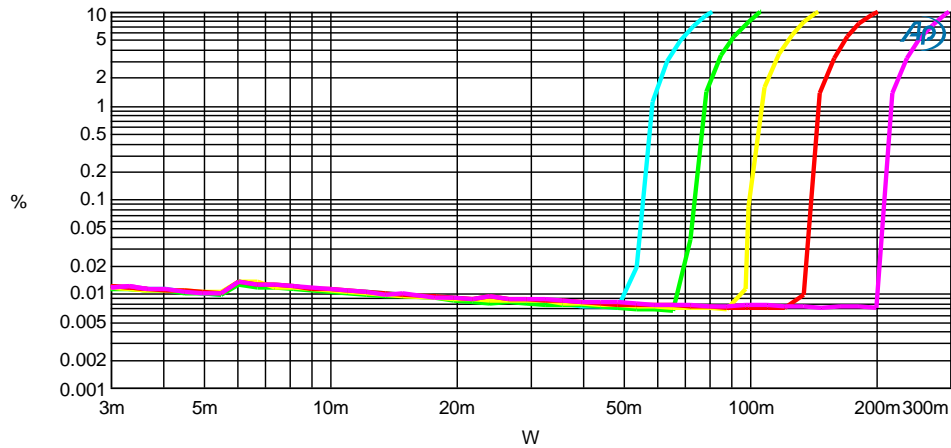


Note 2: Measurement bandwidth is 22Hz to 22kHz.

### Typical Operating Characteristic

Audio Precision

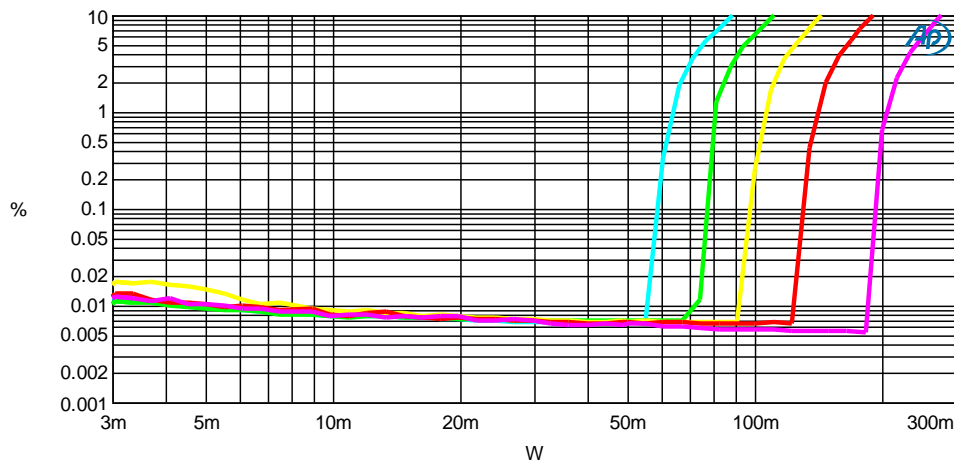
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Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Cyan	Solid	3	Analyzer.THD+N Ratio A	Left	3.0V,16ohm
2	1	Green	Solid	3	Analyzer.THD+N Ratio A	Left	3.3V,16ohm
3	1	Yellow	Solid	3	Analyzer.THD+N Ratio A	Left	3.7V,16ohm
4	1	Red	Solid	3	Analyzer.THD+N Ratio A	Left	4.2V,16ohm
5	1	Magenta	Solid	3	Analyzer.THD+N Ratio A	Left	5.0V,16ohm

Figure 4. THD+N VS Output Power, Freq=1kHz, RL=16Ω

Audio Precision

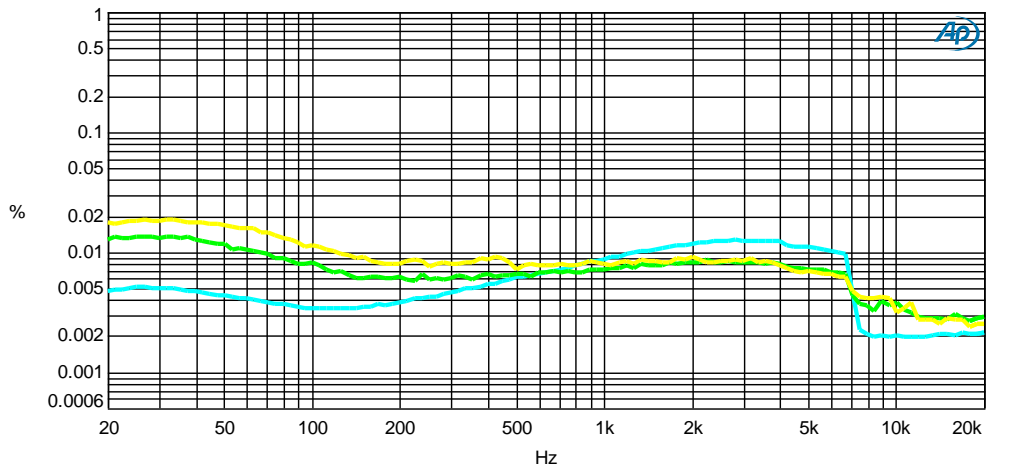


Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Cyan	Solid	3	Analyzer.THD+N Ratio A	Left	3.0V,32ohm
2	1	Green	Solid	3	Analyzer.THD+N Ratio A	Left	3.3V,32ohm
3	1	Yellow	Solid	3	Analyzer.THD+N Ratio A	Left	3.7V,32ohm
4	1	Red	Solid	3	Analyzer.THD+N Ratio A	Left	4.2V,32ohm
5	1	Magenta	Solid	3	Analyzer.THD+N Ratio A	Left	5.0V,32ohm

Figure 5. THD+N VS Output Power, Freq=1kHz, RL=32Ω



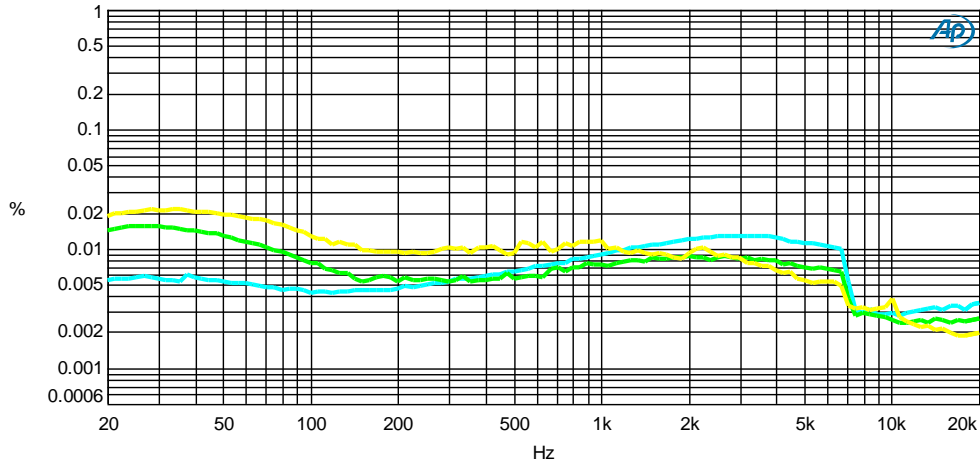
Audio Precision



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Cyan	Solid	3	Analyzer.TH+N Ratio A	Left	PVDD=3V,RL=16ohm,PO=5mW
2	1	Green	Solid	3	Analyzer.TH+N Ratio A	Left	PVDD=3V,RL=16ohm,PO=20mW
3	1	Yellow	Solid	3	Analyzer.TH+N Ratio A	Left	PVDD=3V,RL=16ohm,PO=40mW

Figure 6. THD VS Frequency, PVDD=SVDD=3V, RL=16Ω

Audio Precision

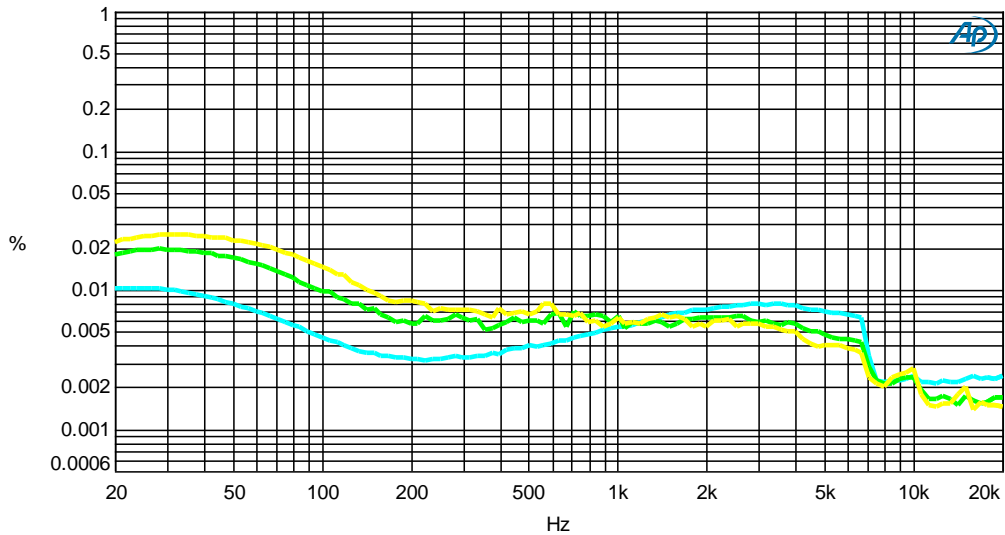


Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Cyan	Solid	3	Analyzer.TH+N Ratio A	Left	PVDD=5V,RL=16ohm,PO=5mW
2	1	Green	Solid	3	Analyzer.TH+N Ratio A	Left	PVDD=5V,RL=16ohm,PO=20mW
3	1	Yellow	Solid	3	Analyzer.TH+N Ratio A	Left	PVDD=5V,RL=16ohm,PO=80mW

Figure 7. THD VS Frequency, PVDD=SVDD=5V, RL=16Ω



Audio Precision

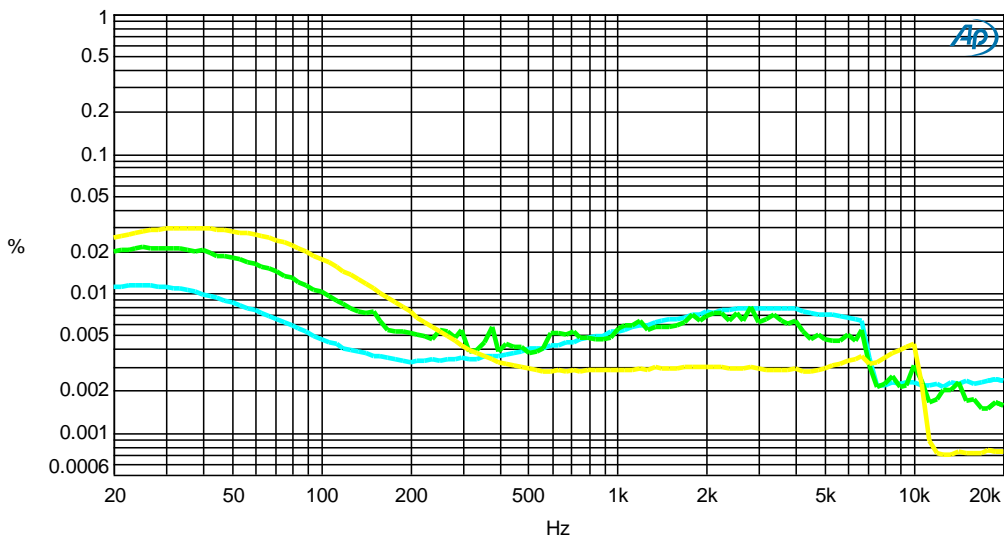


Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Cyan	Solid	3	Analyzer.TH+N Ratio A	Left	3V,32ohm,5mW
2	1	Green	Solid	3	Analyzer.TH+N Ratio A	Left	3V,32ohm,20mW
3	1	Yellow	Solid	3	Analyzer.TH+N Ratio A	Left	3V,32ohm,40mW



Figure 8. THD VS Frequency, PVDD=SVDD=3V, RL=32Ω

Audio Precision

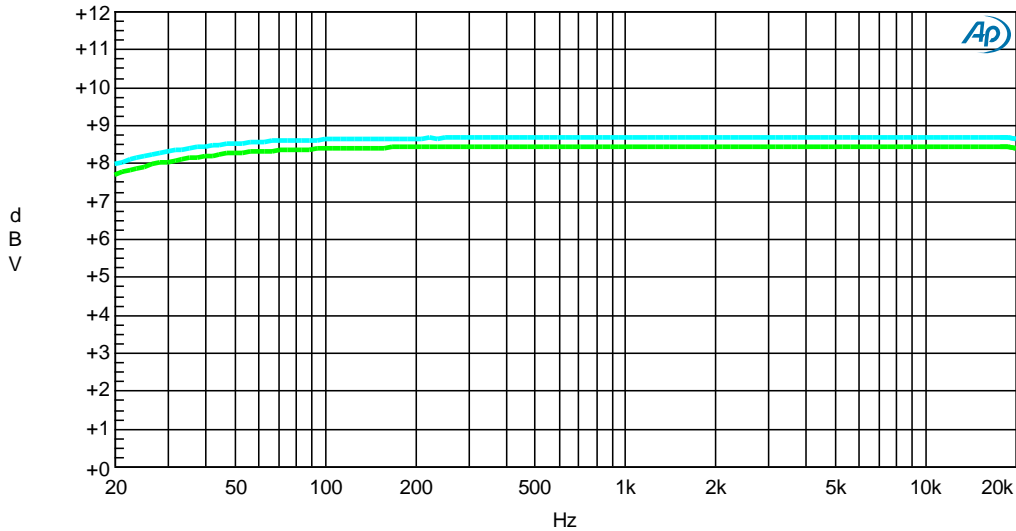


Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Cyan	Solid	3	Analyzer.TH+N Ratio A	Left	5V,32ohm,5mW
2	1	Green	Solid	3	Analyzer.TH+N Ratio A	Left	5V,32ohm,20mW
3	1	Yellow	Solid	3	Analyzer.TH+N Ratio A	Left	5V,32ohm,80mW

Figure 9. THD VS Frequency, PVDD=SVDD=5V, RL=32Ω



Audio Precision



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Cyan	Solid	3	Analyzer.Level A	Left	PVDD=5V,RL=32ohm,THD=1%
2	1	Green	Solid	3	Analyzer.Level A	Left	PVDD=5V,RL=32ohm,THD=0.1%

Figure 10. Output Amplitude VS Frequency, PVDD=SVDD=5V, RL=32 Ω

## Application Information

### Maximum Gain

The LPA4732 has two internal amplifier stages. The first stage's gain is externally configurable, while the second stage's is internally fixed. The closed-loop gain of the first stage is set by selecting the ratio of  $R_f$  to  $R_i$  while the second stage's gain is fixed at 2x. The output of amplifier 1 serves as the input to amplifier 2, thus the two amplifiers produce signals identical in magnitude, but different in phase by 180°. Consequently, the differential gain for the IC is

$$A_v = 20 \log [2 \cdot R_f / (R_i + 10K)]$$

$$R_f = 10 \text{ k } \Omega \pm 10\%$$

### Input Coupling Capacitors

Input coupling capacitors block any DC bias from the audio source and ensure maximum dynamic range. Input coupling capacitors also minimize LPA4732 turn-on pop to an inaudible level.

The input capacitors are in series with LPA4732 internal input resistors, creating a high-pass filter. The following Equation calculates the high-pass filter corner frequency.

$$f = \frac{1}{2\pi R_{IN} C_{IN}}$$





### Charge Pump Flying Capacitor, HPVDD Capacitor and HPVSS Capacitor

The LPA4732 uses a built-in charge pump to generate a positive and negative voltage supply for the headphone amplifiers. The charge pump flying capacitor connects between CAP+ and CAP-. It transfers charge to generate the positive and negative supply voltage. The HPVDD capacitor or HPVSS capacitor must be at least equal in or larger than value to the flying capacitor to allow maximum charge transfer. Use low equivalent-series-resistance (ESR) ceramic capacitors (X5R material or better is required for best performance) to maximize charge pump efficiency. Typical values are 1uF for the HPVDD, HPVSS and flying capacitors.

### Power Supply Decoupling Capacitors

The LPA4732 TureCapFree headphone amplifier requires adequate power supply decoupling to ensure that output noise and total harmonic distortion (THD) remain low. Use good low equivalent-series-resistance (ESR) ceramic capacitors (X5R material or better is required for best performance). Place a 2.2uF capacitor within 5 mm of the PVDD pin. Reducing the distance between the decoupling capacitor and PVDD minimizes parasitic inductance and resistance, improving LPA4732 supply rejection performance. Use 0402 or smaller size capacitors if possible.

### Power Supply Sequencing

Use input coupling capacitors to ensure inaudible turn-on pop. Activate the LPA4732 after all audio sources have been activated and their output voltages have settled. On power-down, deactivate the LPA4732 before deactivating the audio input source. The EN pin controls device shutdown: Set to 0.6 V or lower to

deactivate the LPA4732; set to 1.0 V or higher to activate.

### Layout Recommendations

#### Exposed PAD On LPA4732

Solder the exposed metal pad on the LPA4732 TQFN package to the landing pad on the PCB. Connect the landing pad to ground or leave it electrically unconnected(floating). Do not connect the landing pad to PVDD or to any other power supply voltage. If the pad is grounded, it must be connected to the same ground as the PGND pin 9. Soldering the thermal pad is required for mechanical reliability and enhances thermal conductivity of the package.

### GND Connections

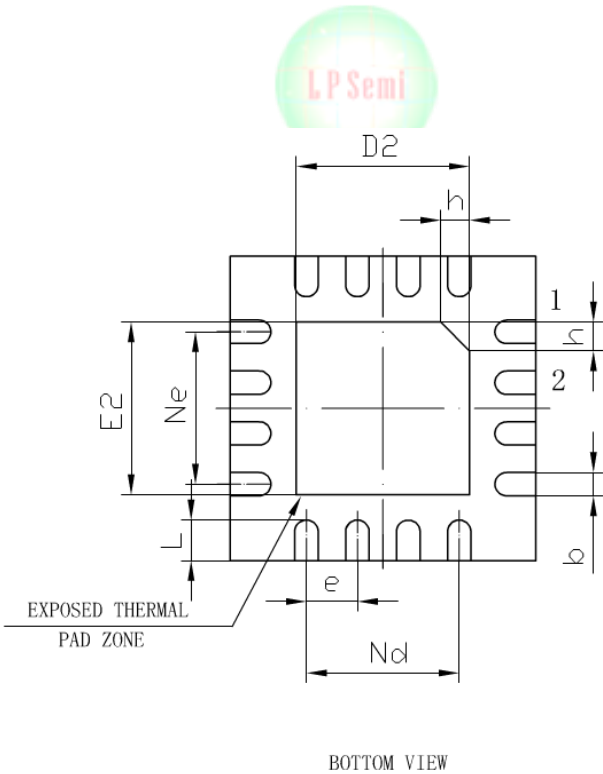
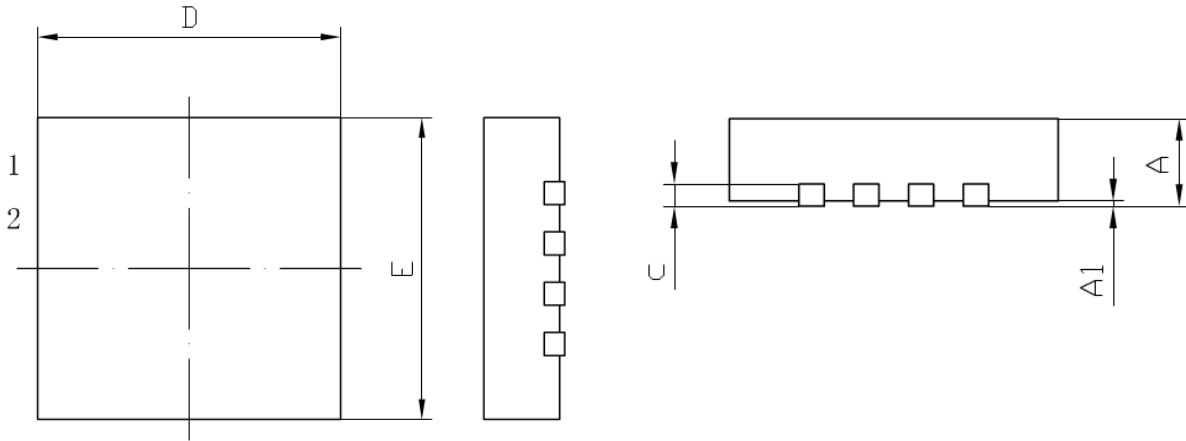
The SGND pin is an input reference and must be connected to the headphone ground connector pin. This ensures no turn-on pop and minimizes output offset voltage. Do not connect more than  $\pm 0.3$  V to SGND.

PGND is a power ground. Connect supply decoupling capacitors for PVDD, HPVDD, and HPVSS to PGND.



Packaging Information

TQFN-16



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	—	0.02	0.05
b	0.18	0.25	0.30
c	0.18	0.20	0.25
D	2.90	3.00	3.10
D2	1.55	1.65	1.75
e	0.50BSC		
Ne	1.50BSC		
Nd	1.50BSC		
E	2.90	3.00	3.10
E2	1.55	1.65	1.75
L	0.35	0.40	0.45
h	0.20	0.25	0.30