Fast Charging Interface Physical Layer IC

General Description

The LP103S is a fast charge protocol controller. The feature monitors USB D+/D- data line's signal, and automatically adjusts output voltage of power source output to optimize charge time.

The LP103S was supported USB Battery Charging Specification Revision 1.2(BC1.2), DCP apply the 2.7V operation function, Spreadtrum Fast Charge Protocol (SFCP), HiSilicon Fast Charge Protocol, Qualcomm® Quick Charge™ 2.0/3.0 Class A and B.

Other features include output over voltage protection, output under voltage protection, temperature sensor detector and under-voltage lockout (UVLO). The LP103S is available in a space saving SOP-8 and SOT23-6 package.

Order Information

LP103S□□□
- F: Green
- Package Type
  - SO: SOP-8
  - B6 : SOT-23-6

Features

- Power consumption below 1mW@5 V
- Support USB BC1.2
- Supports USB DCP 2.7V
- Supports QC2.0 Class A and Class B
- Supports QC3.0 Class A and Class B
- Support HiSilicon FCP Protocol
- Support Spreadtrum SFCP Protocol
- Support Samsung Mode
- Under-Voltage Protection
- Output Over-Voltage Protection
- Output Short-Circuit Protection
- Remote Shutdown Protection
- Over-Temperature Protection
- UL Certification No. 4787974756
- Certificate of Spreadtrum
- Available in SOP-8 and SOT23-6
- RoHS Compliant and Halogen Free

Applications

- Battery Charge Port
- USB Dedicated Charging Port
- Wall-Adapter

Marking Information

Device	Marking	Package	Shipping
LP103S	LPS LP103S YWX	SOP-8	4K/REEL
	LP103S YWX	SOT23-6	3K/REEL
Y: Year code. **W**: Week code. **X**: Series number.			

Typical Application Circuit

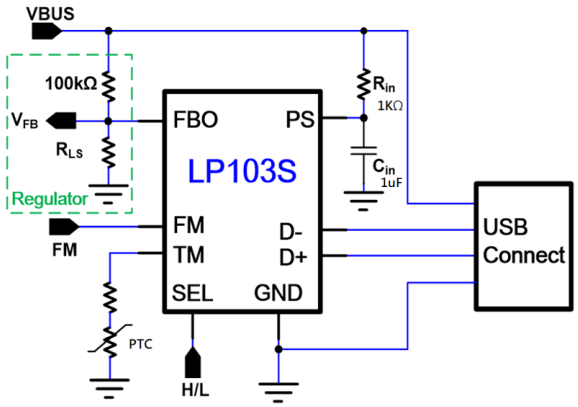


Figure 1A. Typical Application Circuit of LP103S with SOP-8 Package Type.

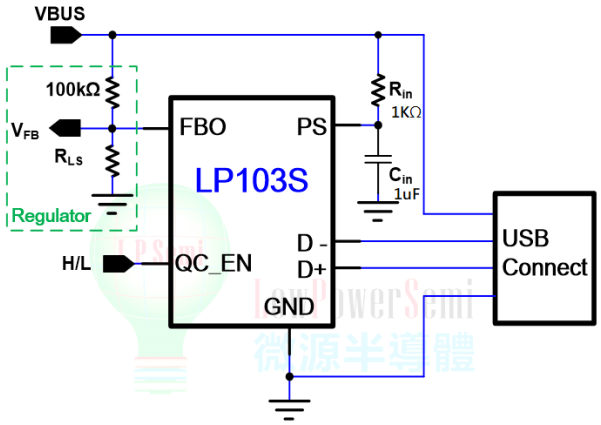


Figure 1B. Typical Application Circuit of LP103S with SOT23-6 Package Type.

Note 1. Recommend adding a 200kΩ resistor from D+ to GND for MI4 application

Pin Configuration

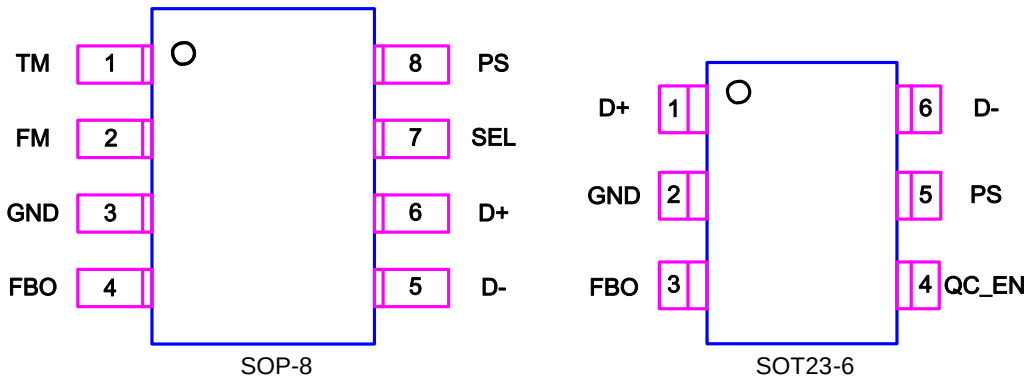


Figure 2. Pin Configuration (Top View)

Function Block Diagram

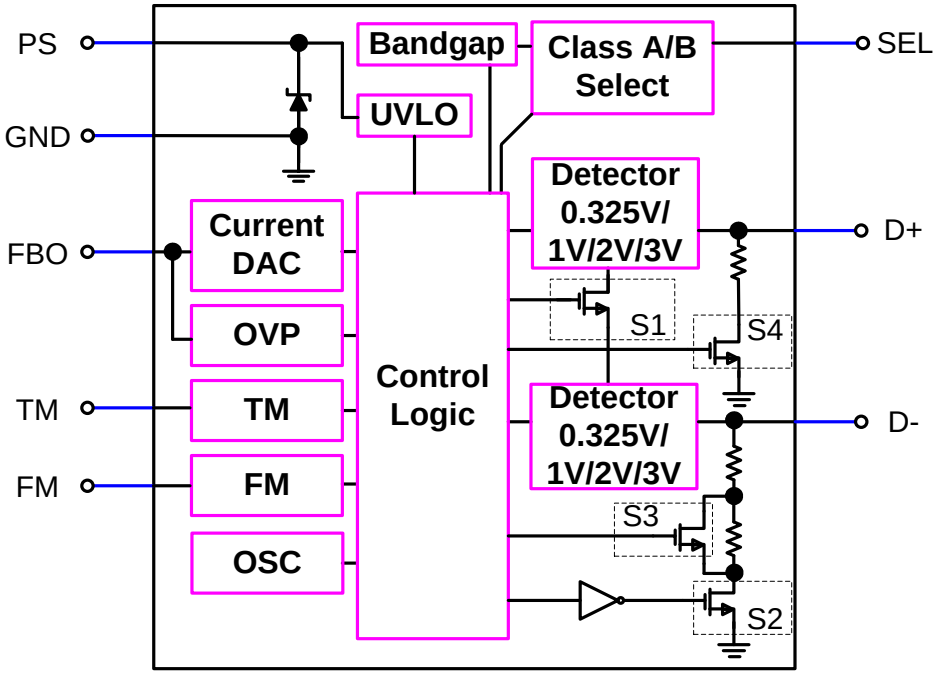


Figure 3. Function Block Diagram

Functional Pin Definition

Pin NO.	SOP8	SOT23-6	Description
TM	1	--	Temperature Monitor. Optional external temperature sensor connection point.
FM	2	--	Fault Monitor. Protection mode output driving external shutdown circuitry in case a fault is detected.
GND	3	2	Ground.
FBO	4	3	Feedback loop drive output. Connected to reference input of external power supply error amplifier to set output voltage.
D-	5	6	USB D- data line input.
D+	6	1	USB D+ data line input.
SEL	7	--	Class A/B Selection. Set SEL to low for Class A. Set this pin to high for Class B. Internal pulled low by 1.1MΩ to GND.
PS	8	5	Power Source. Connection point for an external bypass capacitor for the internally generated supply voltage.
QC_EN	--	4	High Voltage Quick Charge Enable. Set QC_EN to low for disable HVQC. Set QC_EN to high for HVQC operation. Internal pulled high by 2uA.

Absolute Maximum Ratings Note2

- ✧ PS to GND ---------- -0.3V to +6.5V
- ✧ D+/D- to GND ---------- -0.3V to +6.5V
- ✧ All Other Pin to GND ---------- -0.3V to +6.5V
- ✧ PS Current ---------- 25mA
- ✧ D+/D- Current ---------- 1mA
- ✧ Operating Junction Temperature Range (T_J) ---------- -40℃ to 150℃
- ✧ Operation Ambient Temperature Range (T_A) ---------- -40°C to +105°C
- ✧ Storage Temperature Range ---------- -65°C to +150°C
- ✧ Maximum Soldering Temperature (at leads, 10sec) ---------- +260°C

Note 2. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Information

- ✧ Thermal Resistance

SOP-8, θ_{JA} ---------- 112°C/W

SOP-8, θ_{JC} ---------- 39°C/W

SOT23-6, θ_{JA} ---------- 99.1°C/W

SOT23-6, θ_{JC} ---------- 67°C/W

Electrical Characteristics

V_{BUS} = 5V, T_A = 25°C, Unless otherwise specified

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply and Reference Function						
Power Source Voltage	V_{PS}	T_J= +25 °C	3.1	4.3	6.3	V
Power-Up Reset Threshold Voltage	$V_{PS(UVLO)}$		2.5	2.7	2.9	V
Power Source Current	I_{PS}	V_{PS}=4.3V, T_J=25°C			200	μA
Power Shunt Voltage	$V_{PS(Shunt)}$	I_{PS}= 8mA		6.2		V
SEL and QC_EN Pin Voltage	V_{IH}	Logic High.	V_{PS}-1V			V
	V_{IL}	Logic Low			1	
SEL Pin Pull Down Resistance	R_{PD}			1.1		MΩ
QC_EN Pull Up Current Source	I_{CS}			2		uA
D+ and D- Data Line Functions (Dedicated Charging Port -- DCP 1.2V/2.7V)						
DCP1.2V Data Line Output Voltage	$V_{DCP1.2V}$		1.08	1.2	1.32	V
DCP1.2V Data Line Output Resistance	$R_{DCP1.2V}$			100		kΩ
DCP2.7V Data Line Output Voltage	$V_{DCP2.7V}$		2.57	2.7	2.84	V
DCP2.7V Data Line Output Resistance	$R_{DCP2.7V}$			33.6		kΩ
D+ and D- Data Line Functions (Spreadtrum Fast Charge Protocol -- SFCP)						
SFCP Detect Voltage	V_{D_VT0}		0.309	0.325	0.34	V
	V_{D_VT1}		0.95	1.00	1.05	V
	V_{D_VT2}		1.90	2.00	2.10	V
	V_{D_VT3}		2.85	3.00	3.15	V
SFCP Mode Glitch Filter Time	T_{G_det}		1.6	2.1	2.6	s
Rise/Fall Voltage Delay Time	$T_{V\_Rise/\ V\_Fall}$				100	ms
Deglitch Time	T_G				3	ms

Electrical Characteristics (Continued)

V_{BUS} = 5V, T_A = 25°C, Unless otherwise specified

Parameter	Symbol	Test Conditions		Min	Typ	Max	Units
D+ and D- Data Line Functions (High Voltage Dedicated Charging Port -- HVDCP)							
Data Detect Voltage	$V_{DAT(REF)}$			0.250	0.325	0.400	V
Output Voltage Selection Reference	$V_{SEL(REF)}$			1.8	2	2.2	V
Data Lines Short-Circuit Delay	$T_{DAT(Short)}$	V_{OUT} ≥ 0.8 V			10	20	ms
D+ High Glitch Filter Time	$T_{G(BC)DONE}$			1		1.5	s
D- Low Glitch Filter Time	$T_{G(DM)Low}$			1			ms
Output Voltage Glitch Filter Time	$T_{G(V)CH}$			20	40	60	ms
Continuous Mode Glitch Filter Time	$T_{G(Cont)CH}$			100		200	µs
D+ Leakage Resistance	$R_{DAT(LXG)}$	V_{PS} = 3.1V~6.3V, V_{D+} = 0.5-3.6V, S1 is Off		300	900	1500	kΩ
D- Pull-Down Resistance	$R_{DM(DWN)}$			14.25	19.53	24.5	kΩ
Switch S1 On-Resistance	$R_{DS(ON)S1}$	V_{PS}= 4.3V, V_{D+} ≤ 3.6V, I_{Drain}=200µA			20	40	Ω
FEEDBACK Pin Drive Functions							
Output Over-Voltage Threshold	$V_{TH(OV)}$	QC2.0 Mode Class A/B	I_{FBO}=0uA (5V)	1.44	1.52	1.60	V
			I_{FBO}=40uA (9V)	1.60	1.72	1.84	
			I_{FBO}=70uA (12V)	1.74	1.87	2.00	
			I_{FBO}=150uA (20V)	2.12	2.28	2.44	
		QC3.0 Mode	Class A	1.74	1.87	2.00	
			Class B	2.12	2.28	2.44	
FBO Source Current Step	ΔI_{FBO}				2		µA
Protection Functions							
Output OV Detection Delay Time	$T_{D(OV)}$				50		µs
Output OV Detection Blanking Time	$T_{B(OV)}$			500			ms
Output Socket Fault Detection Threshold	$V_{TH(PM)}$			0.250	0.325	0.400	V
Socket Fault Detection Delay Time	$T_{D(PM)}$	I_{Clamp} = 100µA			40		ms
FM Clamp Voltage	$V_{TH(FM)}$				1		V
Over-Temperature Detection Threshold	$V_{TH(TM)}$			1.12	1.20	1.28	V
Over-Temperature Detection Delay Time	$T_{D(TM)}$				1		ms
Temperature Monitor Current Source	I_{TM}				100		µA
Temperature Monitor Current On-Time	$T_{ON(ITM)}$				12		ms
Protection Mode Current Source	I_P			100	150	200	µA

Application Information

The LP103S is a fast charge protocol controller. It monitors USB D+/D- data line's signal, and automatically adjusts output voltage of power source output to optimize charge time.

Under Voltage Lockout (UVLO)

The LP103S had an UVLO internal circuit that enable the device once the voltage on the V_{PS} voltage exceeds the UVLO threshold voltage.

Power Source

Connect a 1kΩ resistor from VBUS to PS pin is recommended. It can limit the current flowing into the PS pin and thus into the shunt regulator at the PS pin to less than 8mA to protect chip. there are also recommended a decoupling capacitor through PS pin to GND.

Fault Monitor

It is needed to detect a loaded condition and trigger protection in case of loading in the absence of a portable device.

D+/D- Data Lines

All protocol transients by USB data line.

Temperature Monitor

If additional system level thermal protection is required. According to Over Temperature Detection Threshold Voltage $V_{TH(TM)}$ and Temperature Monitor Current (I_{TM}), the appropriate PTC thermistor can be selected for over-temperature protection.

Feed Back Output

Set the output voltage by selecting the resistive voltage divider ratio. The voltage divider drops the output voltage to the system feedback voltage. Fixed 100kΩ with high-site divider resistor. Determine the low-side resistor R1 by the equation:

$$V_{BUS} = (100k \div R_{LS}+1)\times V_{FB}$$

Class A/B Selection

The LP103S has an output voltage levels selection pin, which allows users to set operational class A or B. Connecting SEL pin to High-Level, users may operate the device at class B. When working with a class A, connect SEL pin to ground or leave it floating as SEL pin with internal pull-down resistance.

QC Enable

For high current and low voltage application, there are good solution to solve it by pull-low QC_EN Pin. It will disable Qualcomm® Quick Charge™ 2.0/3.0 function. When working with QC 2.0/3.0, connect QC_EN to high or leave it floating as QC_EN pin is equipped with internal 2uA pull high currant.

Quickly Charger 2.0/3.0 Interface

At power-up LP103S turns on switch S1 to check short-circuiting USB data lines D+ and D- for the initial handshake between DCP and PD as described in the USB BC1.2 specification. After the USB BC 1.2 handshake is completed, LP103S will turn off switch N1 if it detects a Quick Charge 2.0 or Quick Charge 3.0 compliant PD. Upon completion of the Quick Charge 2.0 and Quick Charge 3.0 handshakes, LP103S will turn on switch S2 and S3 connecting a resistor pull-down resistor to D-.

PD		LP103S	
D+	D-	VBUS Output	Note
0.6V	0.6V	12V	Class A / B
3.3V	0.6V	9V	Class A / B
0.6V	3.3V	Continuous Mode with ±0.2V step	Class A / B
3.3V	3.3V	20V	Class B
0.6V	GND	5V	Default mode

Layout Consideration

The proper PCB layout and component placement are critical for all circuit. Here are some suggestions to the layout of LP103S design.

1. Connected all ground together with one uninterrupted ground plane, which include power ground and analog ground.

2. The input capacitor should be located as closed as possible to the VPS and ground plane.

3. The FBO pin of LP103S is connected to the FB pin of regulator and close placement of two ICs is recommended.

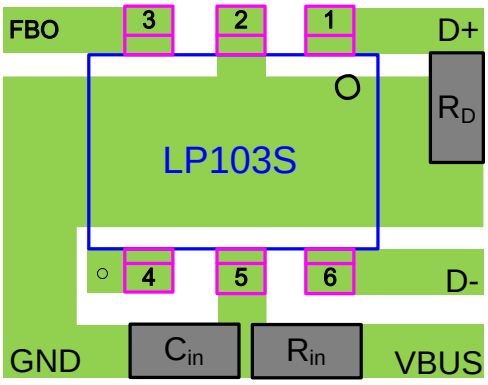
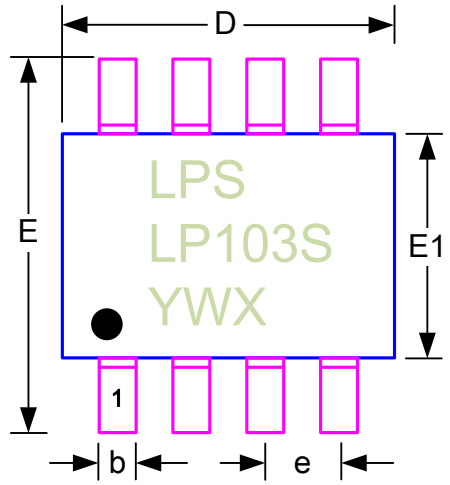


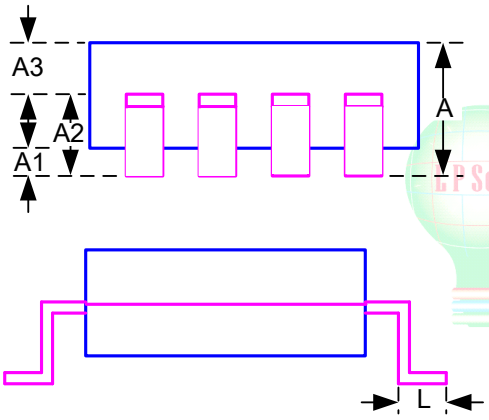
Figure 4. Recommended PCB Layout Diagram

Package Information

SOP-8 Package (Unit: mm)

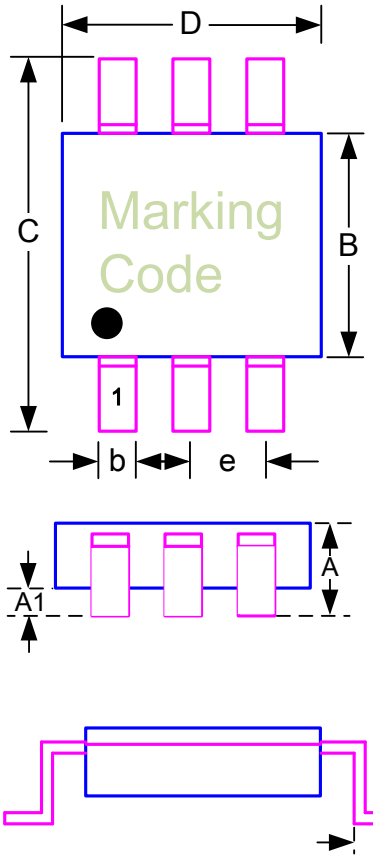


SYMBOL	DIMENSION IN MILLIMETER		
	MIN	NOM	MAX
A	--	--	1.750
A1	0.100	--	0.225
A2	1.300	1.400	1.500
A3	0.600	0.650	0.700
b	0.390	--	0.470
D	4.800	4.900	5.000
E	5.800	6.000	6.200
E1	3.800	3.900	4.000
e	1.27 BSC		
L	0.500	--	0.800



Package Information (Continued)

SOT23-6 Package (Unit: mm)



SYMBOL	DIMENSION IN MILLIMETER	
	MIN	MAX
A	0.700	1.000
A1	0.000	0.100
B	1.397	1.803
b	0.300	0.559
C	2.591	3.000
D	2.692	3.099
e	0.838	1.041
H	0.080	0.254
L	0.300	0.610