Charger Interface Physical Layer IC

General Description

LPS100 is a low-cost USB high-voltage dedicated charging port (HVDCP) interface IC for the Quick Charge 2.0 specification. It incorporates all necessary functions to add Quick Charge 2.0 capability to Power Integrations' switcher ICs such as TOP Switch or Tiny Switch and other solutions employing traditional feedback schemes. LPS100 supports the full output Voltage range of either Class A or Class B. Optionally Class B can be inhibited for protecting the battery charger from accidental damage. LPS100 automatically detects whether a connected Powered Device (PD) is Quick Charge 2.0 capable before enabling output Voltage adjustment. If a PD not compliant to Quick Charge 2.0 is detected the LPS100 disables output Voltage adjustment to ensure safe operation with legacy 5V only USB PDs.

Features

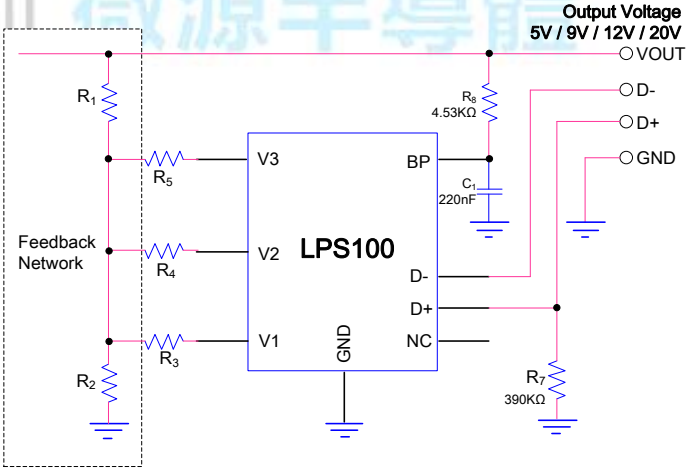
- Fully supports Quick Charge 2.0 specification
  - Class A: 5V, 9V, and 12V output Voltage
  - Class B: 5V, 9V, 12V, and 20V output Voltage
- USB battery charging specification revision 1.2 compatible
- Automatic USB DCP shorting D+ to D- line
- Default 5V mode operation
- Supports TOP Switch and Tiny Switch
- Very low power consumption
  - Below 1mW at 5V output
- Fail safe operation
  - Adjacent pin-to-pin short-circuit fault
  - Open circuit pin fault

Ordering Information

LPS100 □ □ □

- F: Pb-Free
- Package Type
  - SO: SOP-8

Typical Application Circuit



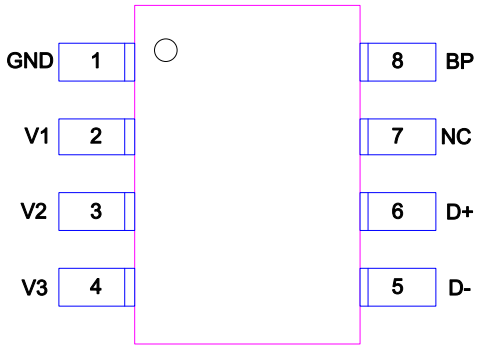
Applications

- Battery chargers for smart phones, tablets
- Net books, digital cameras
- Blue tooth accessories
- USB power output ports

Marking Information

Device	Marking	Package	Shipping
LPS100SOF	LPS LPS100 YWX	SOP-8	4K/REEL
Marking indication: Y:Production year W:Production week X:Series number			

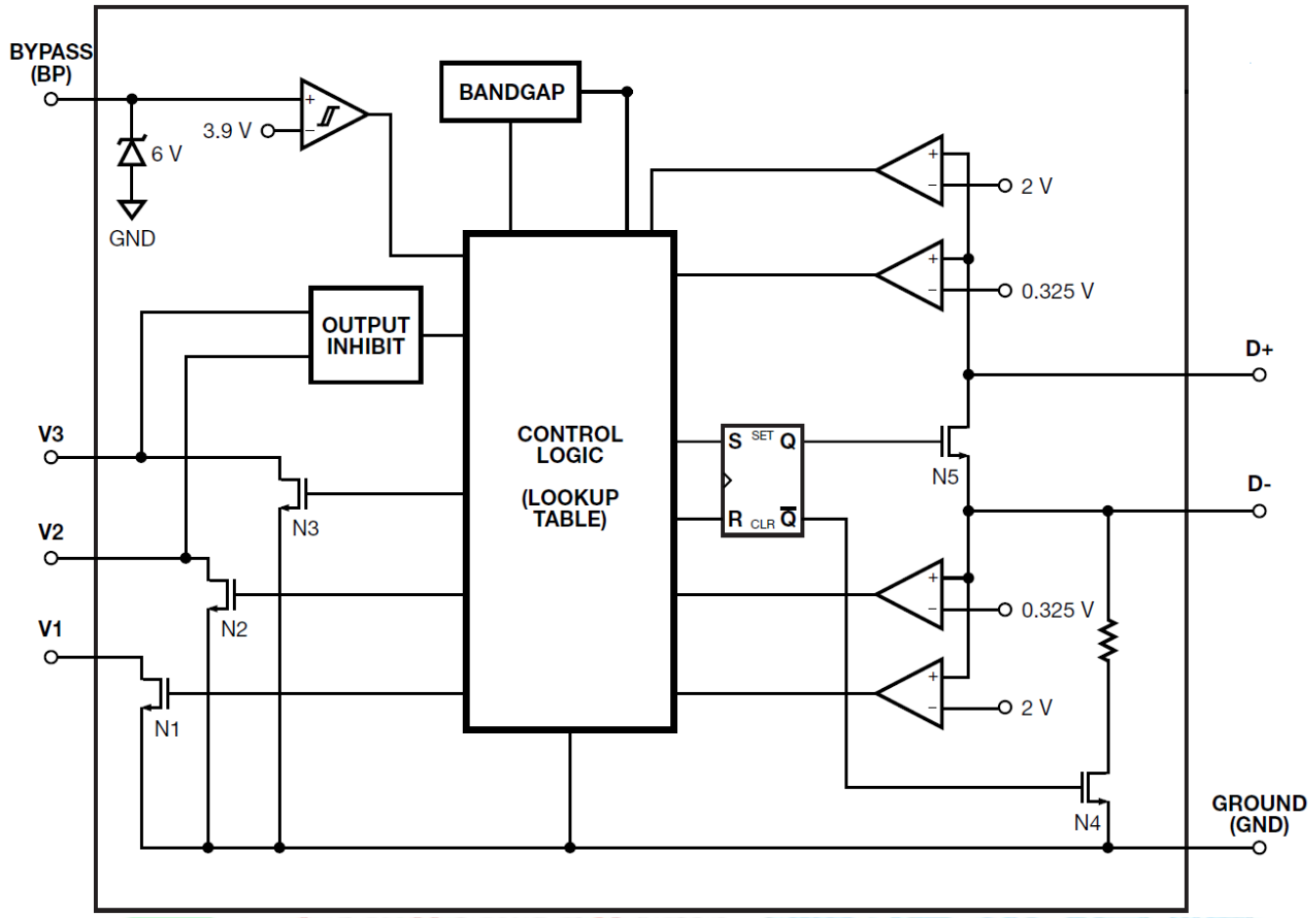
Pin Configurations



Functional Pin Description

Pin No.	Pin Name	Description
1	GND	Ground Pin.
2	V1	Open Drain input of output Voltage adjustment switch. Active for 9V, 12V, and 20V output setting.
3	V2	Open Drain input of output Voltage adjustment switch. Active for 12V, and 20V output setting.
4	V3	Open Drain input of output Voltage adjustment switch. Active for 20V output setting.
5	D-	USB D- data line input.
6	D+	USB D+ data line input.
7	NC	No connection.
8	BP	Connection point for an external bypass capacitor for the internally generated supply Voltage.

Function Block Diagram



Absolute Maximum Ratings

- ✧ BYPASS Pin Voltage ---------- -0.3V to +9V
- ✧ REFERENCE Pin Voltage ---------- -0.3V to +9V
- ✧ V1/V2/V3 Pin Voltage ---------- -0.3V to +9V
- ✧ D+/D- Pin Voltage ---------- -0.3V to +5V
- ✧ BYPASS Pin Current ---------- 25mA
- ✧ V1/V2/V3 Pin Current ---------- 0.5mA
- ✧ D+/D- Pin Voltage ---------- 1mA
- ✧ Operating Junction Temperature ---------- -40°C to +150°C
- ✧ Operating Ambient Temperature---------- -10°C to +105°C
- ✧ Storage Temperature---------- -65°C to +150°C
- ✧ Lead Temperature---------- 260°C

Electrical Characteristics for Each Channel

(SOURCE = 0V; TJ = -20 °C to +85 °C (Unless Otherwise Specified))

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply, Reference and Protection Functions						
BYPASS Pin Voltage	V_{BP}		4	5	6	V
Power-Up Reset Threshold Voltage	$V_{BP(RESET)}$		2.0		3.9	V
BYPASS Pin Source Current	I_{BPSC}	V_{BP} = 4.3V, T_J = 25 °C N1 = N2 = N3 = Off			135	μA
BYPASS Pin Shunt Voltage	$V_{BP(SHUNT)}$	I_{BP} = 3mA	5.7	6	6.3	V
HVDCP Functions						
Data Detect Voltage	$V_{DAT(REF)}$		0.25	0.325	0.4	V
Output Voltage Selection Reference	$V_{SEL(REF)}$		1.8	2	2.2	V
12V / 20V Output Inhibit Threshold	V_{INH}		V_{BP} -0.6			V
Data Lines Short-Circuit Delay	$T_{DAT(SHORT)}$	V_{OUT} ≥ 0.8V		10	20	ms
D+ High Glitch Filter Time	$T_{GLITCH(BC)DONE}$		1000	1250	1500	ms
Output Voltage Glitch Filter Time	$T_{GLITCH(V)CHANGE}$		20	40	60	ms
D- Pull-Down Resistance	$R_{DM(DWN)}$		14.25	19.53	24.5	kΩ
Switch N1 On-Resistance	$R_{DS(ON)N1}$	I_{N1} = 200μA			300	Ω
Switch N2 On-Resistance	$R_{DS(ON)N2}$	I_{N2} = 200μA			300	Ω
Switch N3 On-Resistance	$R_{DS(ON)N3}$	I_{N3} = 200μA			300	Ω
Switch N4 On-Resistance	$R_{DS(ON)N4}$	I_{N4} = 200μA			300	Ω
Switch N5 On-Resistance	$R_{DS(ON)N5}$	I_{N5} = 200μA,$V_{(D+)}$ ≤ 3.6V		20	40	Ω
Data Line Capacitance	$C_{DCP(PWR)}$	Guaranteed by design. Not tested in production.			1	nF

Operation Information

LPS100 is a low-cost USB high-voltage dedicated charging port (HVDCP) interface IC for the Quick Charge 2.0 specification. It incorporates all necessary functions to add Quick Charge 2.0 capability to Power Integrations' integrated switcher ICs such as TOPSwitch or TinySwitch. LPS100 also supports other solutions with traditional feedback schemes like optocoupler and secondary reference regulator TL431 as depicted in Figure 1.

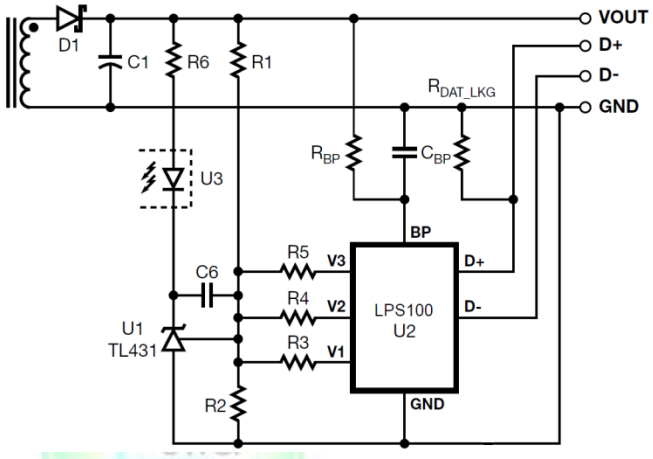


Figure 1. LPS100 with Traditional Output Regulation (CV Only).

LPS100 supports the full output Voltage range of Quick Charge 2.0 Class A (5V, 9V, or 12V) or Class B (5V, 9V, 12V, or 20V). It automatically detects either Quick Charge 2.0 capable powered devices (PD) or legacy PDs compliant with the USB Battery Charging Specification revision 1.2 and only enables output Voltage adjustment accordingly.

Shunt Regulator

The internal shunt regulator clamps the BYPASS pin at 6V when current is provided through an external resistor (RBP in Figure 1). This facilitates powering of LPS100 externally over the wide power supply output Voltage range of 5V to 20V. Recommended Values are RBP = 4.53kΩ and CBP = 220nF.

BYPASS Pin Undervoltage

The BYPASS pin undervoltage circuitry resets the LPS100 when the BYPASS pin Voltage drops below 3.9V. Once the BYPASS pin Voltage drops below 3.9V it must rise back to 4V to enable correct operation.

Quick Charge 2.0 Interface

At power-up LPS100 turns on switch N5 (see Figure 3) in 20ms or less after the BYPASS pin Voltage has reached 4V. Switch N4 and output switches N1 to N3 remain off. This sets the default 5V output Voltage level. With D+ and D- short-circuited the normal handshake between the AC-DC adapter (DCP) and powered devices (PD) as described in the USB Battery Charging Specification 1.2 can commence. After switch N5 has been turned on LPS100 starts monitoring the Voltage level at D +. If it continuously stays above 0.325V for at least 1.25 seconds LPS100 will enter Quick Charge 2.0 operation mode. If the Voltage at D+ drops any time below 0.325V LPS100 resets the 1.25 seconds timer and stays in USB Battery Charging Specification 1.2 compatibility mode with a default output Voltage of 5V.

Once LPS100 has entered Quick Charge 2.0 operation mode switch N5 will be turned off. Additionally switch N4 is turned on connecting a 19.53kΩ pull-down resistor to D-. As soon as the Voltage at D- has dropped low (<0.325V) for at least 1ms LPS100 starts accepting requests for different AC-DC adapter output Voltages by means of applied Voltage levels at data lines D+ and D- through the powered device. Table 1 summarizes the output Voltage lookup table, corresponding AC-DC adapter output Voltages and status of switches N1 to N3.

D+	D-	Output	Switch Status
0.6V	0.6V	12V	N1 = N2 = On, N3 = Off
3.3V	0.6V	9V	N1 = On, N2 = N3 = Off
3.3V	3.3V	20V	N1 = N2 = N3 = On
0.6V	GND	5V(Default)	N1 = N2 = N3 = Off

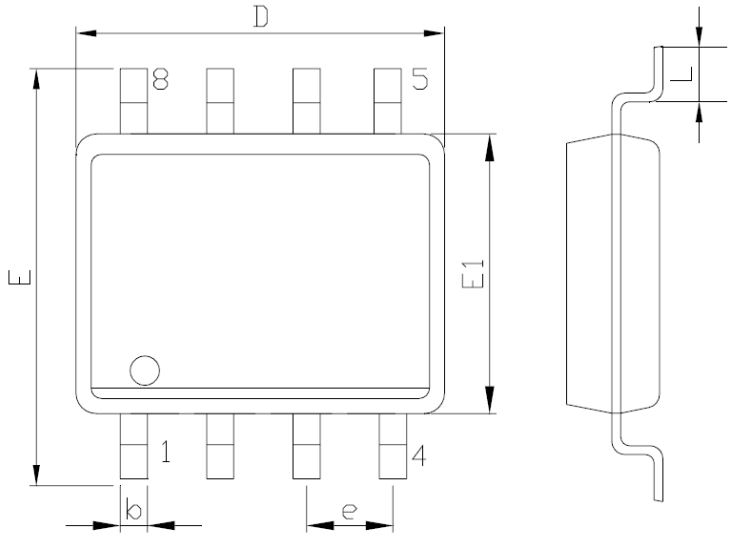
Table 1. Output Voltage Lookup Table。

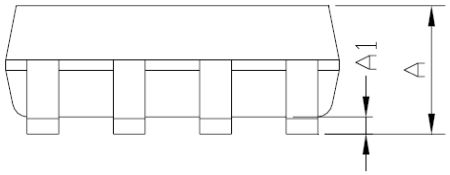
Requests made by a connected powered device to set a 12V output Voltage can be inhibited by connecting theV2 pin to the BYPASS pin (either directly or through a resistor up to 100kΩ). This will also inhibit requests for a 20V output. Connecting theV3 pin to BYPASS (directly or through a resistor up to 100kΩ) will inhibit any requests for setting a 20V output.

At USB cable disconnect the Voltage level at D+ is pulled down by resistor $R_{DAT(LKG)}$ (see Figure 1). Once it drops below 0.325V LPS100 will turn on switch N5 (thereby short-circuiting D+ and D-) and turns off switches N1 to N4. This sets the default output Voltage of 5V. The recommended Value for $R_{DAT(LKG)}$ = 390kΩ.

Packaging Information

SOP-8





SYMBOLS	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
D	4.90		0.193	
E	5.80	6.20	0.228	0.244
E1	3.90		0.153	
L	0.40	1.27	0.016	0.050
b	0.31	0.51	0.012	0.020
e	1.27		0.050	