LPA4890

1.2W Filter-free Mono Audio Power Amplifier

Features

- 2.5-5.5V Operation Voltage
- 0.1μA Ultra-low Current Shutdown Mode
- Improved Pop & Click Circuitry
- Unique Modulation Scheme Reduces EMI Emissions
- No Output Filter Required
- External Gain Configuration Capability
- 0.4V Compatible Threshold for /SHDN Pin
- BTL Output Supporting Capacitive Loads
- RoHS Compliant and 100% Lead(Pb)-Free
- Package: MSOP-8

Applications

- PMP
- PSP
- Game Machine
- GPS Tracker
- Portable Electronic Devices

General Description

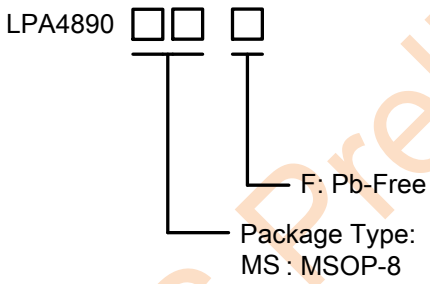
The LPA4890 is an audio power amplifier designed for portable communication device applications such as GPS trackers. The LPA4890 is capable of delivering 1.2W of continuous average power to an 8Ω load from a 5.2V power supply with less than 1% distortion (THD+N).

The LPA4890 is designed specifically to provide high quality output audio power with a minimal number of external components. The LPA4890 does not require output coupling capacitors or bootstrap capacitors, and therefore is ideally suited where minimal board or solution size is a primary requirement. It features a low-power shutdown mode, which is achieved by driving the /SHDN pin with logic low. Additionally, the LPA4890 features an internal thermal shutdown protection.

The LPA4890 contains circuitry to prevent “pop and click” noise that would occur during turn-on and turn-off transitions. For maximum flexibility, the LPA4890 provides an externally controlled gain (with resistors), as well as an externally controlled turn-on and turn-off times (with the bypass capacitor).

The LPA4890 is available in a MSOP-8 package.

Marking Information



Ordering and Package Information

Part Number	Top Mark	Package	T&R
LPA4890MSF	LPA 4890M YWX	MSOP-8	3K/REEL
Marking indication: Y: Production Year, W: Production week, X: Series Number			

Typical Application Circuits

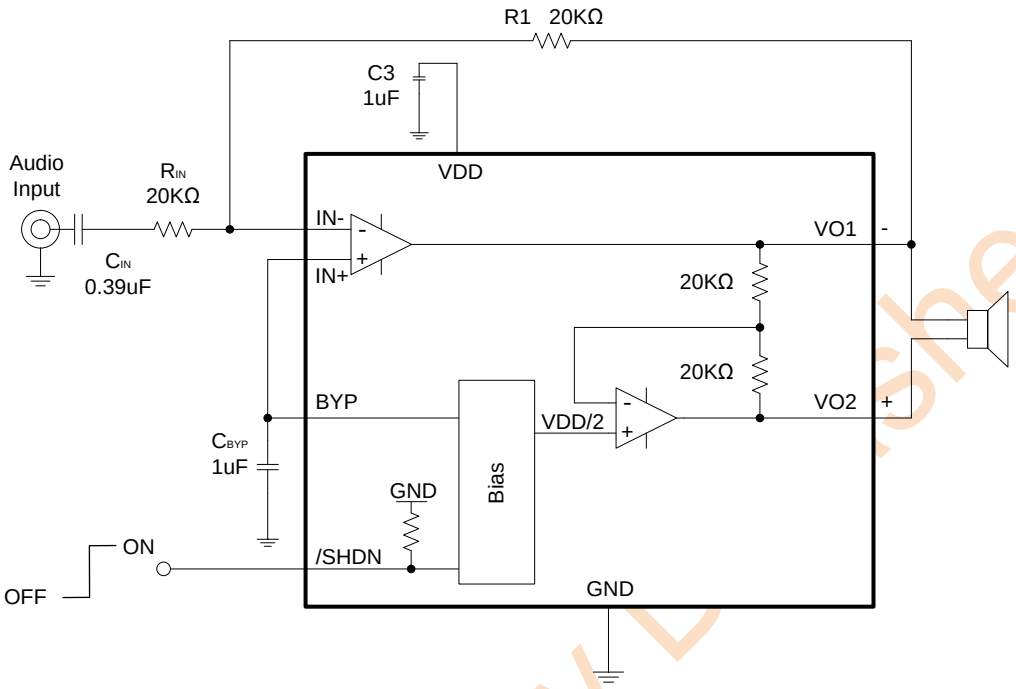


Figure 1-1. Typical Application Circuits with Single Input

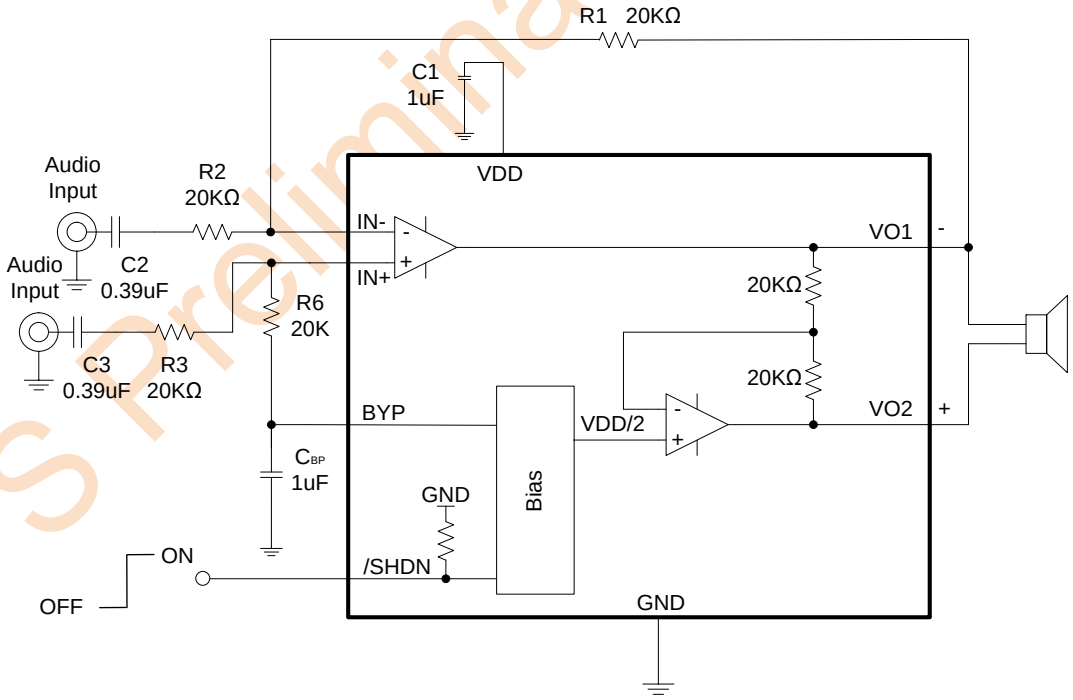
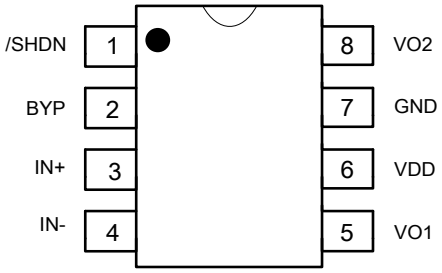


Figure 1-2. Typical Application Circuits with Differential Input

Pin Configuration



MSOP-8 (Top View)

Pin Description

Pin	Name	Description
1	/SHDN	Shutdown input pin. The device is enabled with this pin pulled high. The device enters the shutdown mode if this pin is floating or pulled low. This pin is internally pulled down to GND through the R_{PD} resistor (refer to Figure 2 and Electrical Characteristics Table).
2	BYP	Bypass capacitor pin. This pin provides the common mode voltage. Connect 1μF ceramic capacitor as close as possible to this pin.
3	IN+	Positive input of the first amplifier. This pin receives the common mode voltage.
4	IN-	Negative input of the first amplifier. This pin receives the audio input signal. Connect this pin to the feedback resistor R_F and to the input resistor R_{IN} (refer to Figure 2).
5	VO1	Negative output. Connected this pin to the load and to the feedback resistor R_F.
6	VDD	VDD power supply input. Connect at least 1μF ceramic capacitor as close as possible to this pin.
7	GND	Ground.
8	VO2	Positive output.

Functional Block Diagram

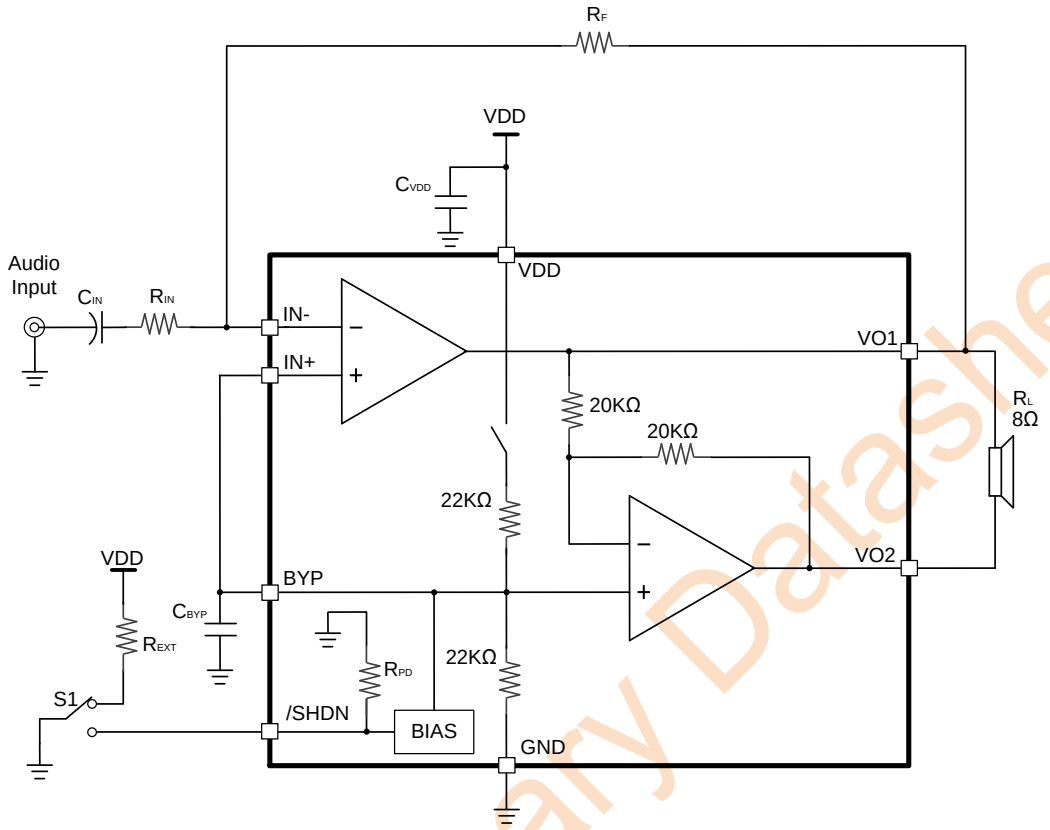


Figure 2. Internal Block Diagram

Absolute Maximum Ratings (Note 1)

- All pins to GND ---------- -0.3V to + 6V
- Maximum Junction Temperature (T_{JMAX}) ---------- 150°C
- Storage Temperature Range, T_{stg} ---------- -65°C to 150°C
- Maximum Soldering Temperature (at leads, 10 seconds) ---------- 260°C

***Note 1: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, instead of functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.**

Thermal Information

- Maximum Power Dissipation (T_A <= 25°C) ---------- 0.9W
- Thermal Resistance (θJA) (Note 2) ---------- 165°C/W

***Note 2: It is based on 2S2P JEDEC standard PCB.**

Recommended Operating Conditions

- Input Voltage ---------- 2.5V to 5.5V
- Ambient Temperature ---------- -20°C to 80°C

Electrical Characteristics

The following parameters are guaranteed under condition V_{DD} =5V, T_A = -40°C to 85°C unless otherwise noted. T_A = 25°C for typical value.

Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
V_{OS}	Output offset voltage (Measured differentially)	V_i=0V, A_v=2V/V, V_{DD}=2.5V to 5.5V			3	20	mV
I_Q	Quiescent current	V_{DD}=5.5V, no load			4.4		mA
		V_{DD}=3.6V, no load			3.4		
		V_{DD}=2.5V, no load			2.9		
I_{SHDN}	Shutdown Current	V_{SHDN}=0.35V, V_{DD}=2.5V to 5.5V			0.1		μA
$R_{DS(ON)}$	Static drain-source on-state resistance	V_{DD}=5.5V, no load			400		mΩ
		V_{DD}=3.6V, no load			500		
		V_{DD}=2.5V, no load			700		
P_o	Output power	V_{DD}=5.2V, R_L=8Ω, THD=1%, f=1KHz			1.2		W
V_{SD_H}	/SHDN pin logic High	V_{DD}=2.5V to 5.5V		1.4			V
V_{SD_L}	/SHDN pin logic Low	V_{DD}=2.5V to 5.5V				0.4	
THD+N	Total harmonic distortion plus noise	V_{DD}=5V, Po=1W, R_L=8Ω, f=1KHz			0.3		%
		V_{DD}=3.6V, Po=0.5W, R_L=8Ω, f=1KHz			0.4		
		V_{DD}=2.5V, Po=0.2W, R_L=8Ω, f=1KHz			0.45		
PSRR	Supply ripple rejection ratio	V_{DD}=5V, inputs ac-grounded with C_i=2uF, V(ripple)=200mV	f=217Hz		-60		dB
			f=1kHz		-62		dB
CMRR	Common mode rejection ratio	V_{DD}=3.6V, V_{ic}=1Vpp	f=217Hz		-62		dB
t_{WU}	Device wake up time	V_{DD}=5V, C_{BYP}=0.1uF			150		ms
R_{PD}	/SHDN pin internal pull-down resistor	V_{DD}=2.5V to 5.5V			290		kΩ

Typical Performance Characteristics

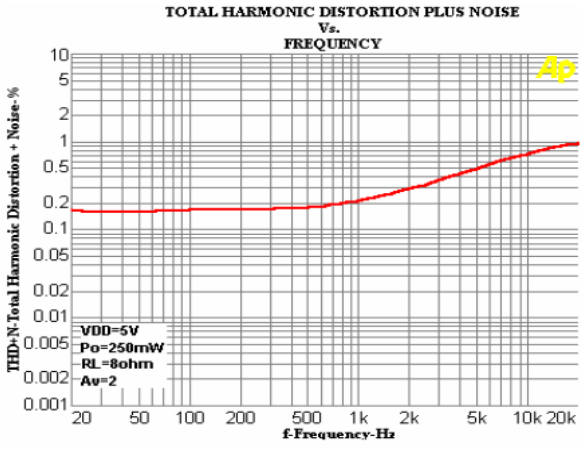


Figure3.

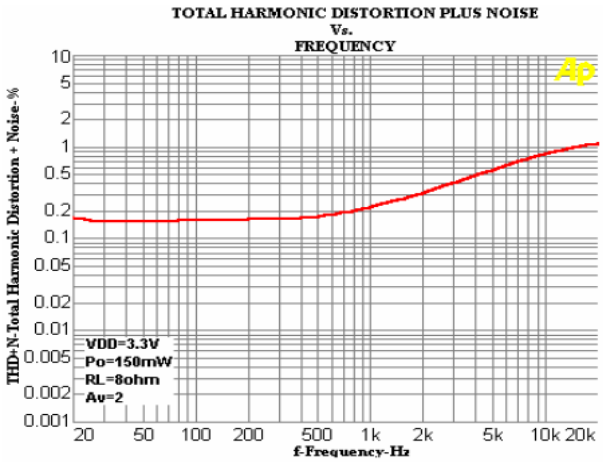


Figure4.

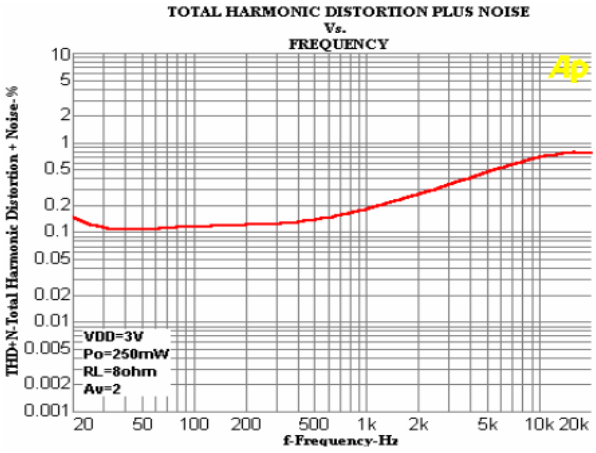


Figure5.

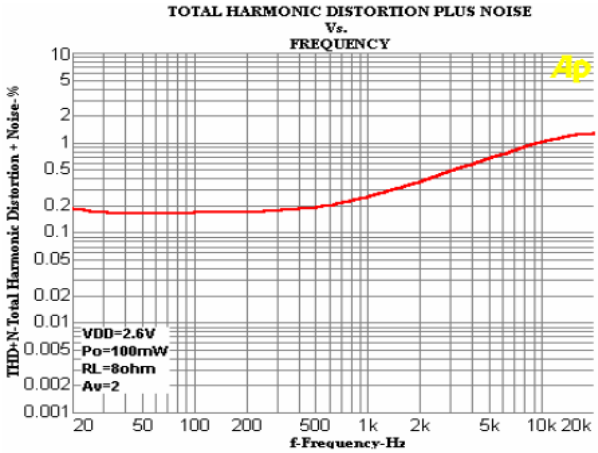


Figure6.

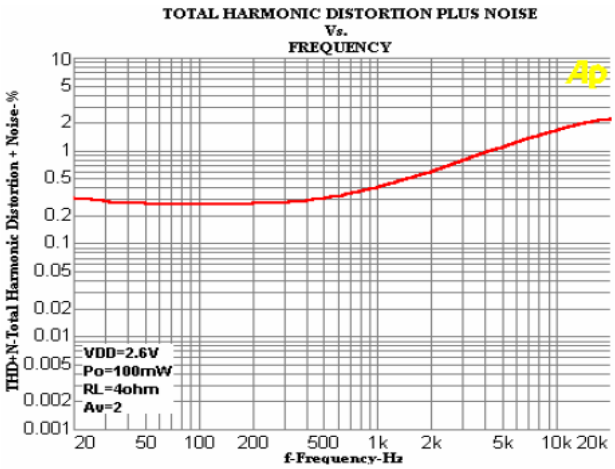


Figure7.

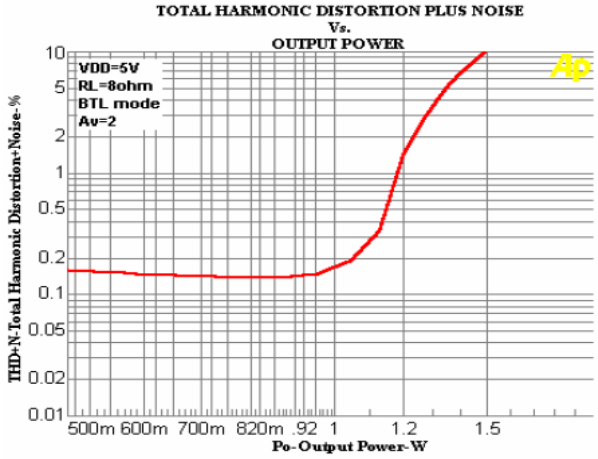


Figure8.

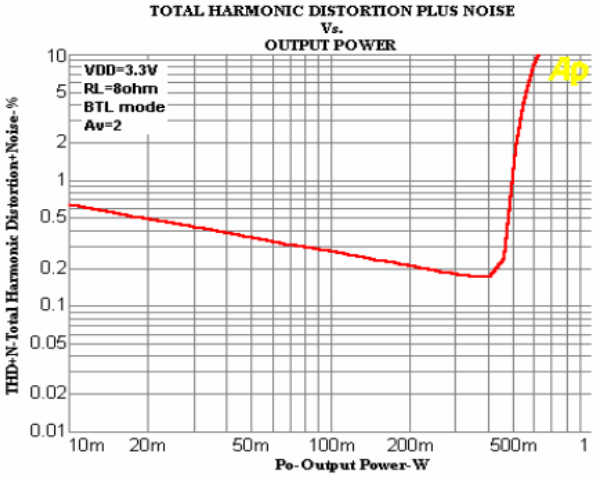


Figure9.

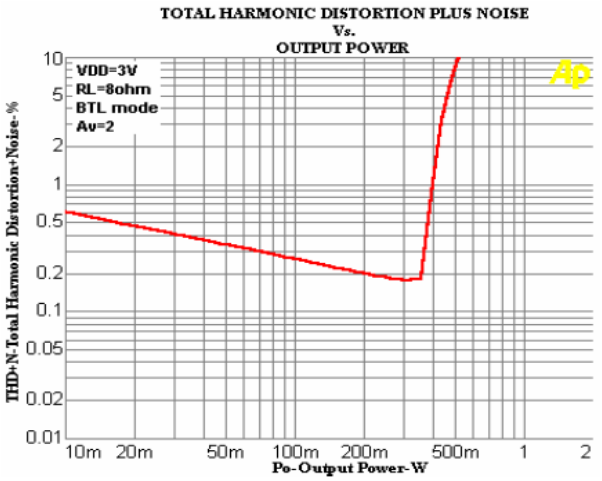


Figure10.

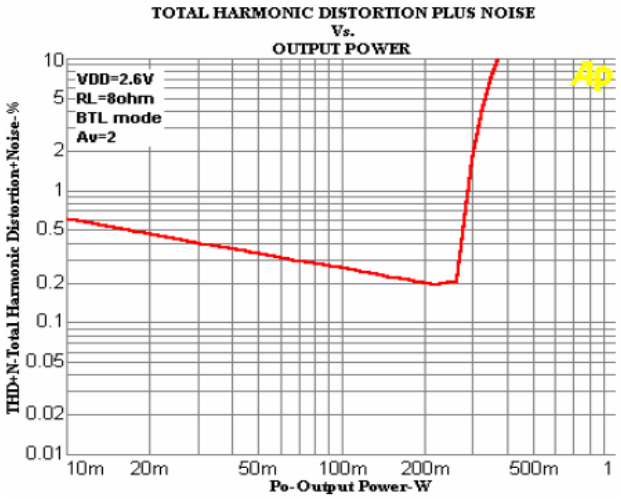


Figure11.

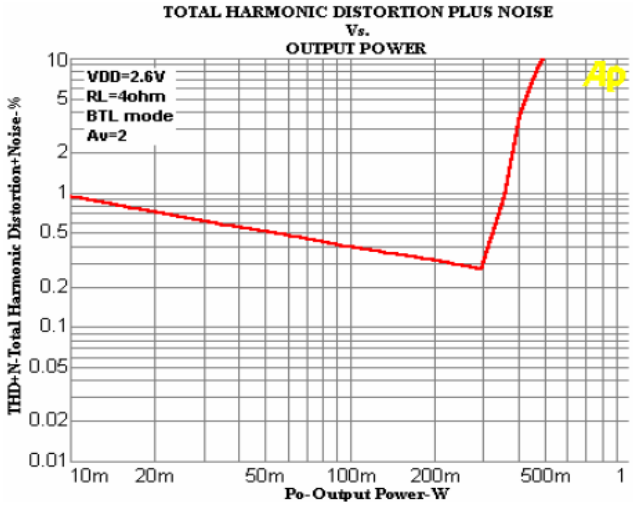


Figure12.

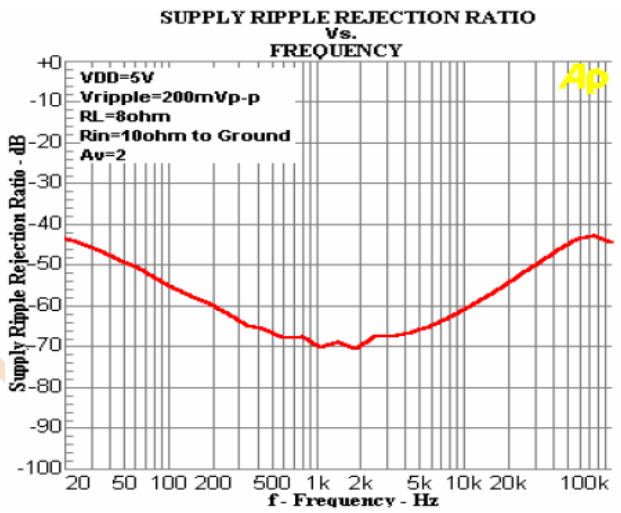


Figure13.

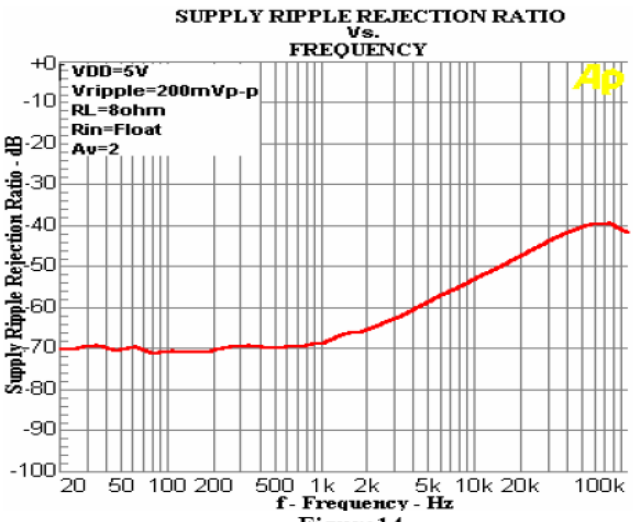


Figure14.

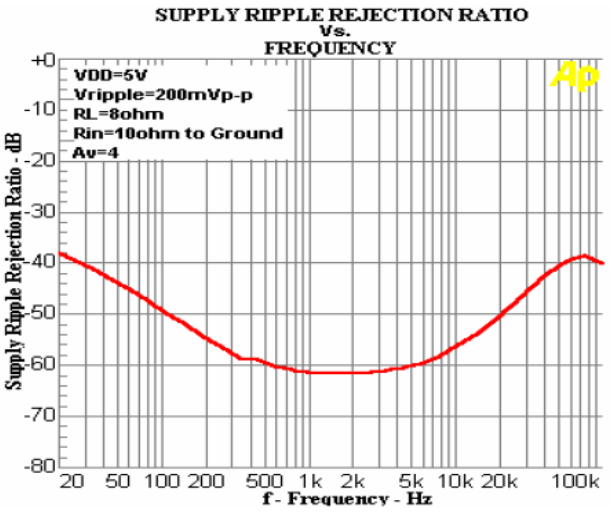


Figure15.

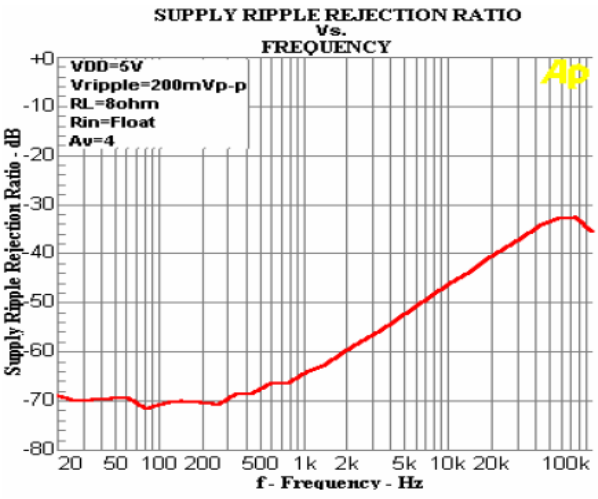


Figure16.

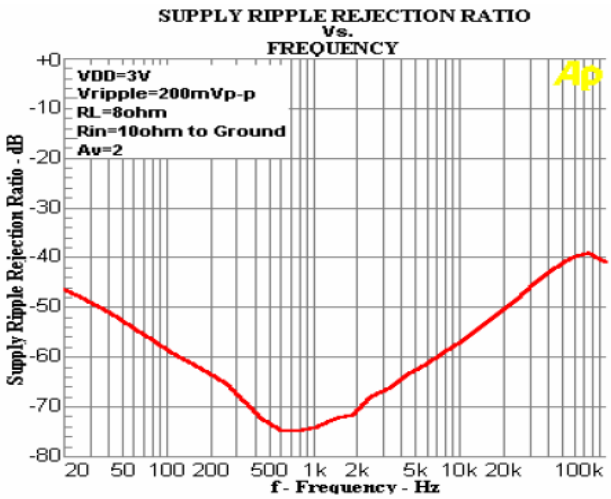
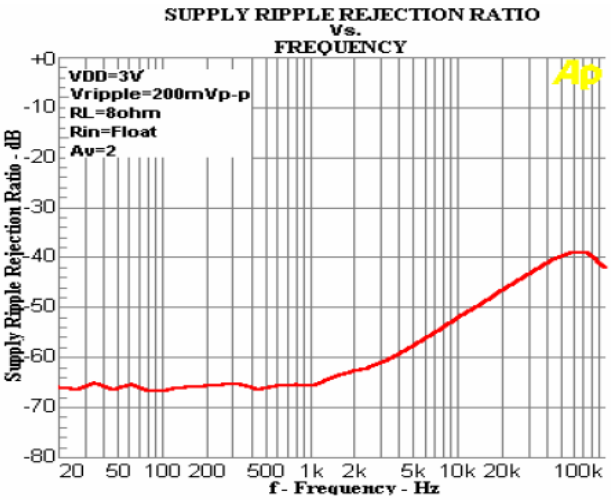


Figure17.



Figue18.

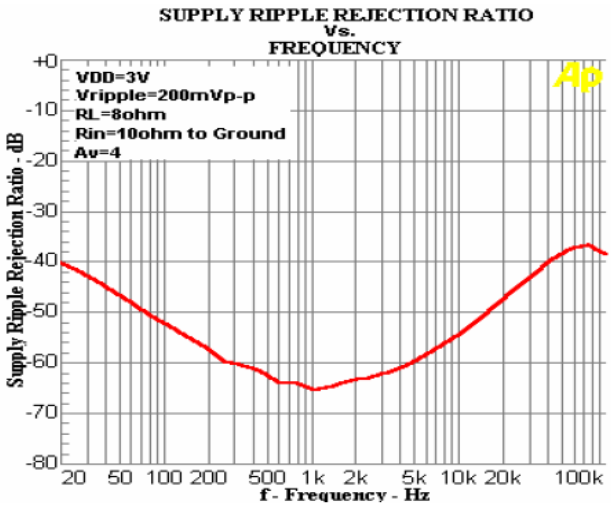


Figure19.

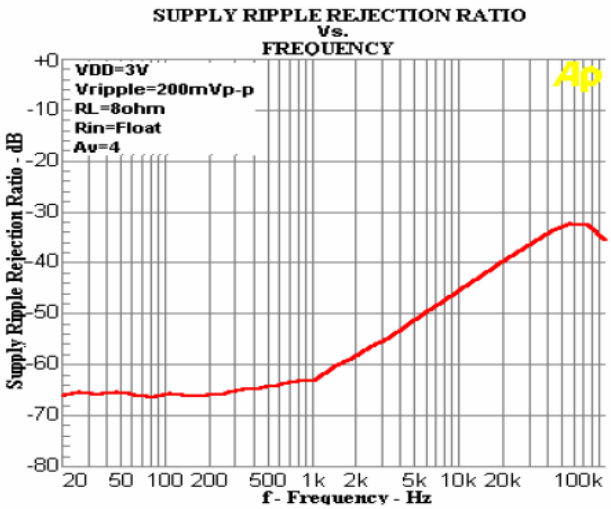


Figure20.

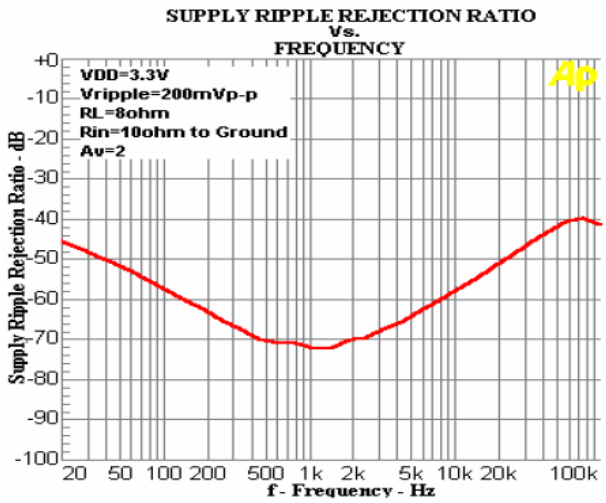


Figure21.

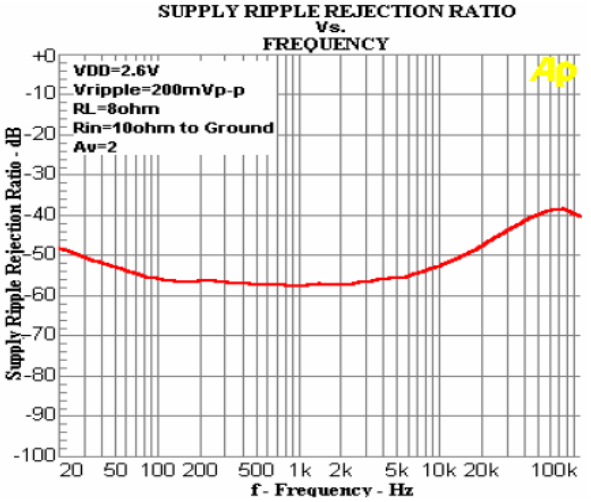


Figure22.

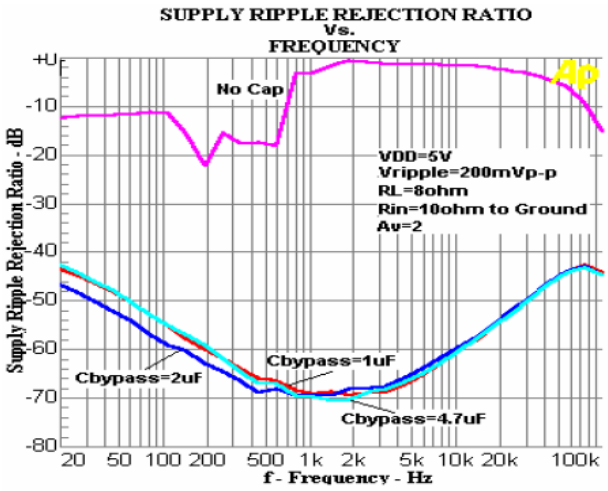


Figure23.

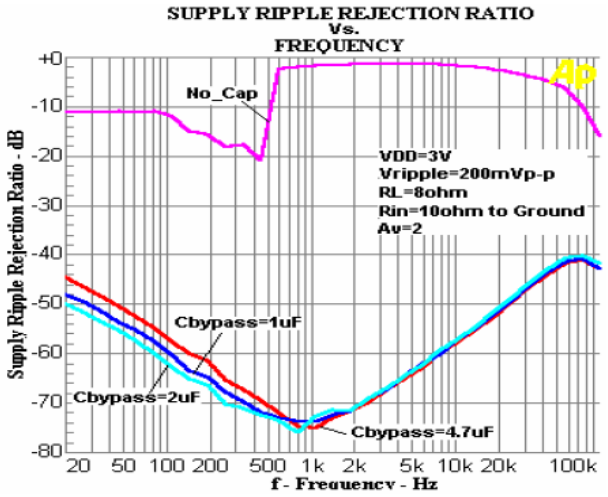


Figure24.

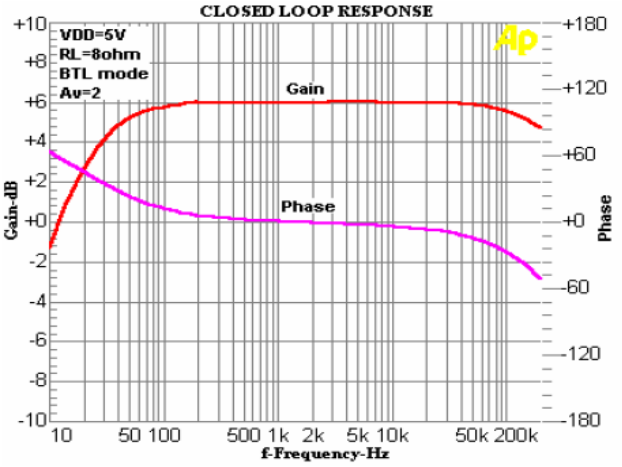


Figure25.

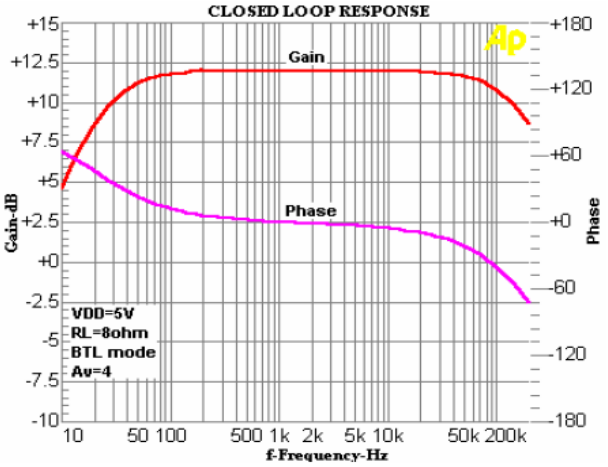


Figure26.

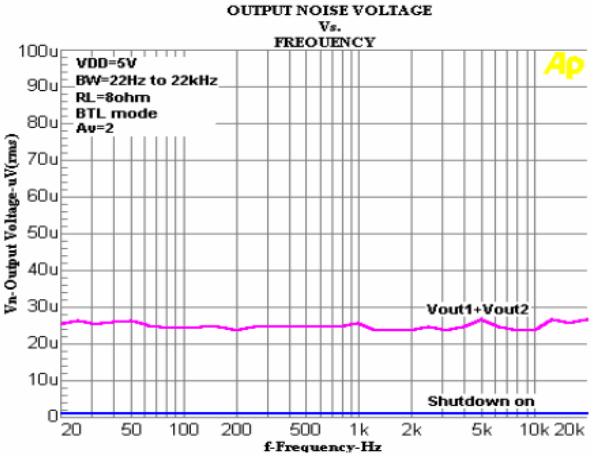


Figure27.

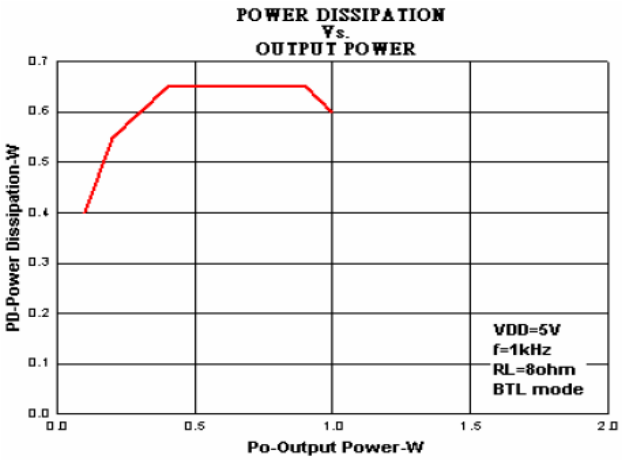


Figure28.

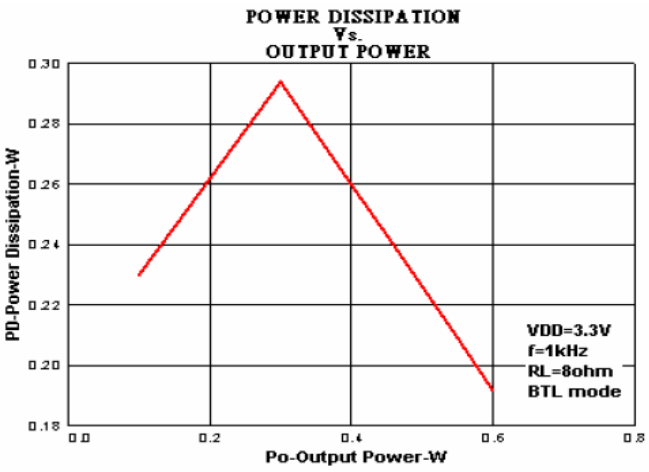


Figure29.

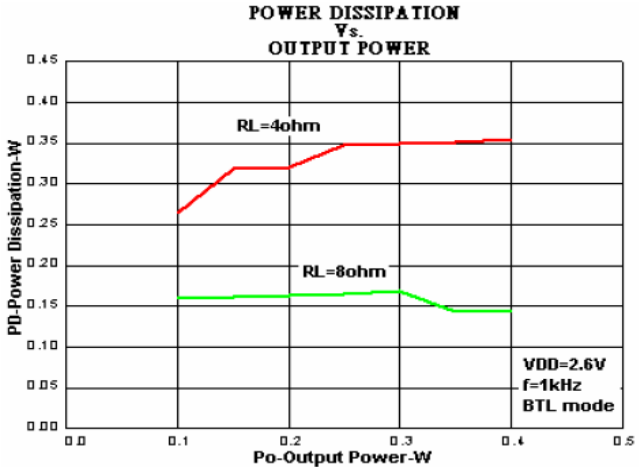


Figure30.

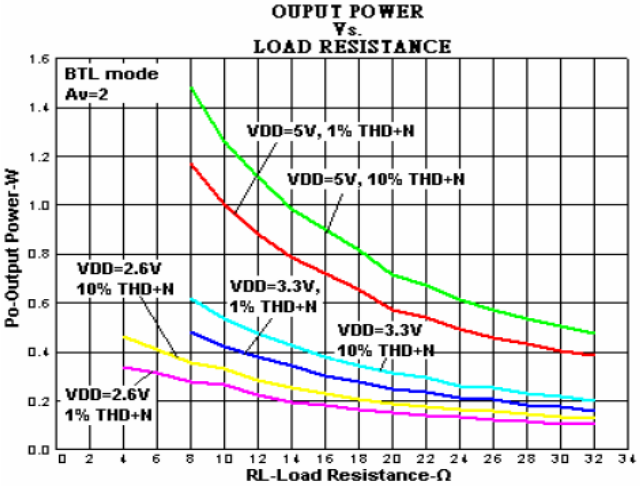


Figure31.

Functional Description

General Description

As shown in Figure 2, the LPA4890 has two operational amplifiers internally, allowing for a few different amplifier configurations. The first amplifier's gain is externally configurable, while the second amplifier is internally fixed in a unity-gain, inverting configuration. The close loop gain of the first amplifier is set by selecting the ratio of R_F to R_{IN} while the second amplifier's gain is fixed by the two internal 20kΩ resistors. Figure 2 shows the output of amplifier one serves as the input to amplifier two, which results in both amplifiers producing signals identical in magnitude, but out of phase by 180°. Consequently, the differential gain A_{VD} for the IC is

$$A_{VD} = 2 \times \frac{R_F}{R_{IN}}$$

By driving the load differentially through outputs VO1 and VO2, an amplifier configuration commonly referred to as “BTL mode” is established. The BTL mode operation is different from the classical single-ended amplifier configuration where one side of the load is connected to ground.

A BTL amplifier design has a few distinct advantages over the single-ended configuration, as it provides differential drive to the load, thus doubling output swing for a specified supply voltage. Four times the output power is possible as compared to a single-ended amplifier under the same conditions. This increase in attainable output power assumes that the amplifier is not current limited or clipped.

A BTL configuration, such as the one used in the LPA4890, also creates a second advantage over single-ended amplifiers. Since the differential outputs, VO1 and VO2, are biased at half-supply, no net DC voltage exists across the load. This eliminates the need for an output coupling capacitor which is required in a single supply, single-ended amplifier configuration. Without an output coupling capacitor, the half-supply bias across the load would result in both increased internal IC power dissipation and also possible loudspeaker damage.

Power Supply Bypassing

As with any amplifier, proper supply bypassing is critical for low noise performance and high-power supply rejection. The capacitor location on both the bypass and power supply pins should be as close to the device as possible. Typical applications employ a 5V regulator with 10 µF tantalum or electrolytic capacitor and a ceramic bypass capacitor that aid in supply stability. This does not eliminate the need for bypassing the supply nodes of the LPA4890. The selection of a bypass capacitor, especially C_{BYP}, is dependent upon PSRR requirements, click and pop performance, system cost, and size constraints.

Shutdown Mode

In order to reduce power consumption while not in use, the LPA4890 contains a /SHDN pin to externally turn off the amplifier. This shutdown feature turns the amplifier off when a logic low is placed on the /SHDN pin. The LPA4890 has an internal pull-down resistor (R_{PD}) on the /SHDN pin, if /SHDN pin is floating, the device will shut down. By switching the /SHDN pin to logic low or pull it down to ground, the LPA4890 supply current draw will be minimized to shutdown current (I_{SHDN}), which is 0.1uA in typical.

Thermal Shutdown

The LPA4890 has thermal shutdown protection to fully protect the device from internally or externally generated excessive temperatures. The thermal shutdown circuit is activated when the die temperature exceeds a safe temperature (typ 170°C) and the switch is turned off. The switch automatically turns on again if the temperature drops below the threshold temperature.

Application Information

Capacitor Consideration

The external capacitor on VDD is recommended in application,1μF for C_{VDD} at least. Closer placement of the capacitors to the device is better for stability.

Shutdown Mode

The device contains a /SHDN pin to externally turn off the amplifier. In many applications, a microcontroller or microprocessor output is used to control the shutdown circuitry to provide a quick, smooth transition into shutdown. Another solution is to use a single-pole, single-throw switch S1 in conjunction with an external pull-up resistor, refer to Figure 2. When the switch connects the /SHDN pin to ground, the amplifier will be disabled. If the switch connects the /SHDN pin to VDD, the device will be enabled. The external pull-up resistor and internal pull-down resistor (R_{PD}) will form a resistor divider, so choose a proper external pull-up resistor is important. Selecting a 10KΩ external pull-up resistor or pulling the /SHDN pin to VDD directly is recommended. This scheme ensures the /SHDN pin in a certain state, thus preventing the unwanted state changes.

Power Dissipation

Power dissipation is a major concern when designing a successful amplifier, whether the amplifier is bridged or single-ended. A direct consequence of the increased power delivered to the load by a bridge amplifier is an increase in internal power dissipation. Since the LPA4890 has two operational amplifiers in one package, the maximum internal power dissipation is 4 times of a single-ended amplifier. The maximum power dissipation for a given application can be derived from below Equation.

$$P_D = 4 * V_{DD}^2 / (2\pi^2 R_L)$$

P_D: Power Dissipation (W)

V_{DD}: Input voltage (V)

R_L: Speaker resistance (Ω)

$$T_J = P_D \times \theta_{JA} + T_A$$

T_J: Junction temperature (°C)

θ_{JA}: Package thermal resistance (°C /W) (Note 3)

T_A: Ambient temperature (°C)

It is critical that the maximum junction temperature T_{JMAX} of 150°C is not exceeded. T_{JMAX} can be determined from the power derating curves by using P_{DMAX} and the PC board foil area. By adding additional copper foil, the thermal resistance of the application can be reduced, resulting in higher P_D. Additional copper foil can be added to any of the leads connected to the LPA4890. If T_{JMAX} still exceeds 150°C, additional changes must be made. These changes can include reduced supply voltage, higher load impedance, or reduced ambient temperature.

***Note 3: The calculation base on thermal resistance is only valid in Lab condition. The value of θ_{JA} could change in customer PCB environment.**

PCB Layout Guidelines

The PCB layout is critical to the optimal performance of an audio amplifier, some general mixed signal layout recommendations for LPA4890 as below:

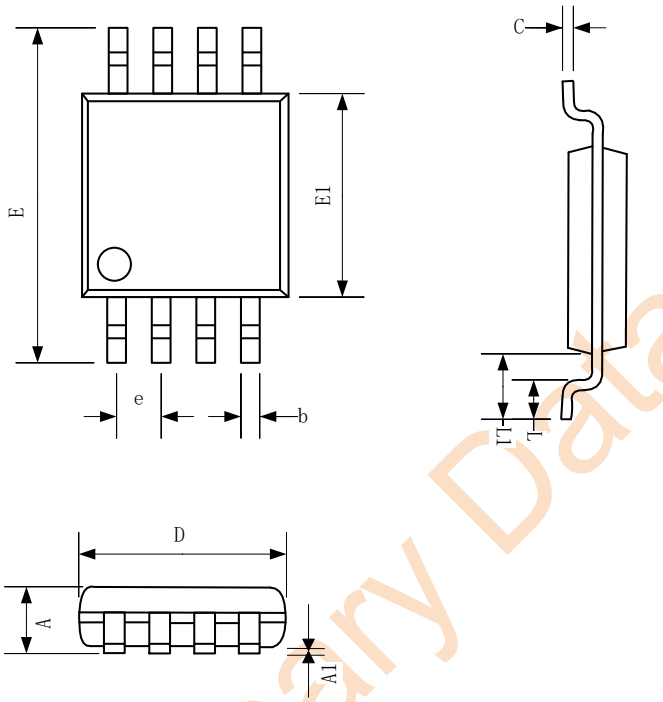
1. Place the C_{VDD} capacitor as close as possible to the device with short, wide traces to the VDD and GND pins.
2. The power ground should be connected to the analog ground through a single point. It is further recommended to put analog and power traces over the corresponding analog and power ground traces to minimize noise coupling.
3. The PCB traces that connect the output pins to the load and the supply pins to the power supply should be as wide as possible to minimize trace resistance, this is helpful to maintain the highest output voltage swing and

corresponding peak output power.

4. Avoid ground loops or running digital and analog traces parallel to each other (side-by-side) on the same PCB layer. Running digital and analog traces at 90 degrees to each other from the top to the bottom side as much as possible will minimize capacitive noise coupling and cross talk.
5. Ensure enough copper area is used for heat sinking to keep the junction temperature below 150°C.

Package Information

MSOP-8



SYMBOL	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	1.10
A1	0.00	-	0.15
b	0.22	0.30	0.38
c		0.17REF	
D	2.90	3.00	3.10
E	4.70	4.90	5.10
E1	2.90	3.00	3.10
e		0.65BSC	
L	0.40	0.60	0.80
L1		0.95 REF	