# LPA4871

3W Filter-free Mono Audio Power Amplifier

## Features

- 2.5-5.5V Operation Voltage
- 0.1μA Ultra-low Current Shutdown Mode
- Improved Pop & Click Circuitry
- Unique Modulation Scheme Reduces EMI Emissions
- No Output Filter Required
- Output Power ($P_O$) at 10% THD+N:

  VDD=5V, 4Ω load, 2.9W(typ)

  VDD=5V, 8Ω load, 1.8W(typ)
- External Gain Configuration Capability
- 0.4V Compatible Threshold for SHDN Pin
- BTL Output Supporting Capacitive Loads
- RoHS Compliant and 100% Lead(Pb)-Free
- Package: SOP-8/MSOP8

## Applications

- GPS Tracker
- PSP
- Game Machine
- Portable Electronic Devices

## General Description

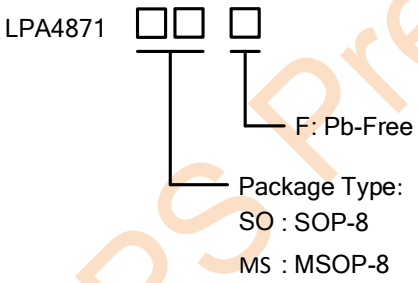
The LPA4871 is an audio power amplifier designed for portable applications such as GPS trackers. The LPA4871 is capable of delivering 3W of continuous average power to a 4Ω load from a 5.2V power supply with less than 10% distortion (THD+N).

The LPA4871 is designed specifically to provide high quality output audio power with a minimal number of external components. The LPA4871 does not require output coupling capacitors or bootstrap capacitors, and therefore is ideally suited where minimal board or solution size is a primary requirement. It features a low-power shutdown mode, which is achieved by driving the SHDN pin with logic high. Additionally, the LPA4871 features an internal thermal shutdown protection.

The LPA4871 contains circuitry to prevent “pop and click” noise that would occur during turn-on and turn-off transitions. For maximum flexibility, the LPA4871 provides an externally controlled gain (with resistors), as well as an externally controlled turn-on and turn-off times (with the bypass capacitor).

The LPA4871 is available in a SOP-8/MSOP8 package.

## Marking Information




## Ordering and Package Information

| Part Number | Top Mark | Package | T&R |
|---|---|---|---|
| LPA4871SOF | LPS<br>LPA4871<br>YWXXX | SOP-8 | 4K/REEL |
| LPA4871MSF | LPS<br>LPA4871<br>YWXXX | MSOP-8 | 3K/REEL |
| Marking indication:<br>Y: Production Year, W: Production week, X: Series Number | | | |

## Typical Application Circuitry

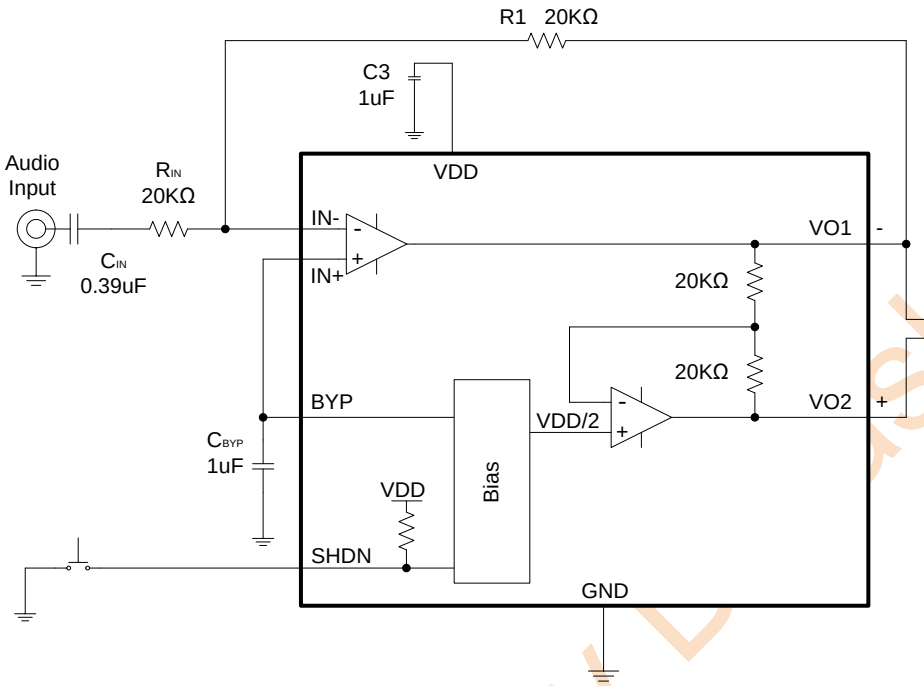



**Figure 1-1. Typical Application Circuits with Single Input**

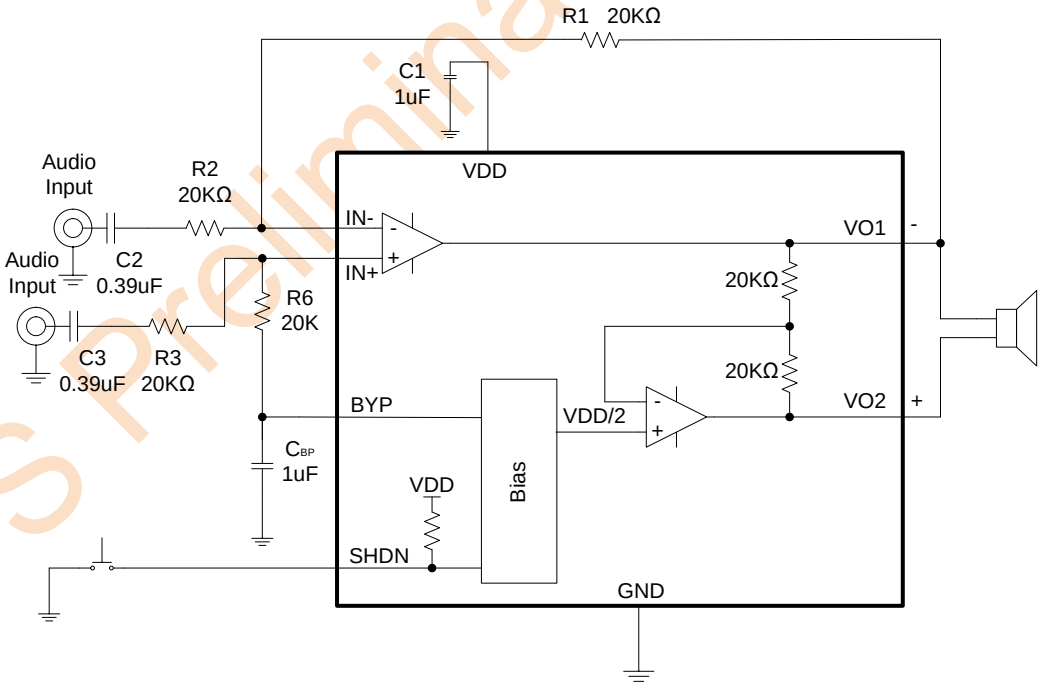
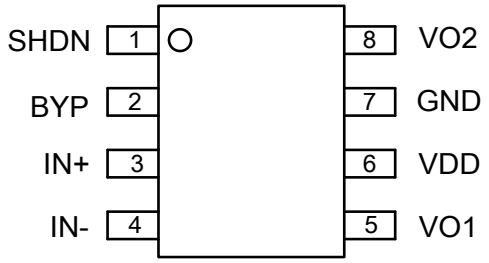



**Figure 1-2. Typical Application Circuits with Differential Input**

## Pin Configuration




(Top View)

## Pin Description

| Pin | Name | Description |
|---|---|---|
| 1 | SHDN | Shutdown input pin. The device is enabled with this pin pulled low. The device enters in shutdown mode if the pin is floating or this pin is pulled high. This pin is internally pulled up to VDD through a 560 kΩ(typ) resistor. |
| 2 | BYP | Bypass capacitor pin. This pin provides the common mode voltage. Connect 1μF ceramic capacitor as close as possible to this pin. |
| 3 | IN+ | Positive input of the first amplifier. This pin receives the common mode voltage. |
| 4 | IN- | Negative input of the first amplifier. This pin receives the audio input signal. Connect this pin to the feedback resistor $R_F$ and to the input resistor $R_{IN}$ (refer to Figure 2). |
| 5 | VO1 | Negative output. Connected this pin to the load and to the feedback resistor $R_F$. |
| 6 | VDD | VDD power supply input. Connect at least 1μF ceramic capacitor as close as possible to this pin. |
| 7 | GND | Ground. |
| 8 | VO2 | Positive output. |

## Functional Block Diagram

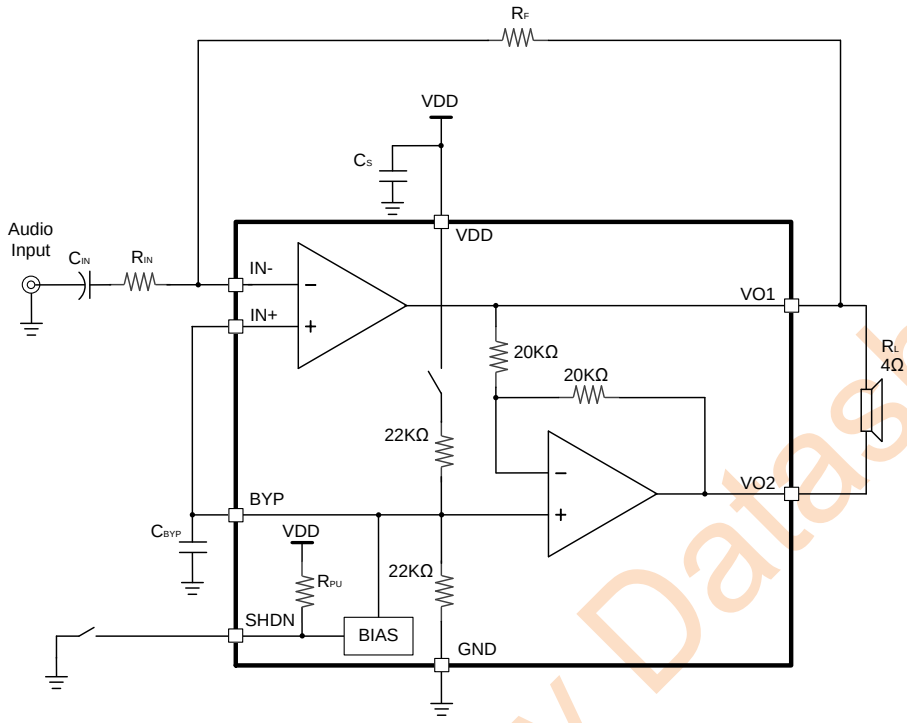



**Figure 2. Internal Block Diagram**

## Absolute Maximum Ratings (Note 1)

- All pins to GND ---------- -0.3V to + 6V
- Maximum Junction Temperature ($T_{JMAX}$) ---------- 150°C
- Storage Temperature Range, Tstg ---------- -65°C to 150°C
- Maximum Soldering Temperature (at leads, 10 seconds) ---------- 260°C

***Note 1: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, instead of functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.**

## Thermal Information

- Maximum Power Dissipation ($T_A$ <= 25°C) ---------- 0.9W
- Thermal Resistance ($\theta_{JA}$) (Note 2) ---------- 140°C/W

***Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by $T_{JMAX}$, $\theta_{JA}$, and the ambient temperature $T_A$. The maximum allowable power dissipation is $P_{DMAX}= (T_{JMAX}–T_A)/ \theta_{JA}$ or the number given in Absolute Maximum Ratings, whichever is lower. For the LM4871, $T_{JMAX}= 150^{\circ}C$. For the $\theta_{JA}$, it is based on 2S2P JEDEC standard PCB.**

## Recommended Operating Conditions

- Input Voltage ---------- 2.5V to 5.5V
- Ambient Temperature ---------- -20°C to 80°C

## Electrical Characteristics

**The following parameters are guaranteed under condition $V_{DD}$ =5V, $T_A$ = -40°C to 85°C unless otherwise noted. $T_A$ = 25°C for typical value.**

| Symbol | Parameter | Test Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{OS}$ | Output offset voltage (Measured differentially) | | | | 2 | 20 | mV |
| $I_Q$ | Quiescent current | $V_{DD}$=5V, no load | | | 4 | | mA |
| $I_{SHDN}$ | Shutdown Current | $V_{SHDN}$=0.35V, $V_{DD}$=2.5V to 5.5V | | | 0.1 | | μA |
| Po | Output power | f=1kHz, $R_L$=4Ω, THD=10% | $V_{DD}$=5V | | 2.9 | | W |
| | | | $V_{DD}$=4.2V | | 2 | | |
| | | | $V_{DD}$=3.7V | | 1.6 | | |
| | | f=1kHz, $R_L$=4Ω, THD=1% | $V_{DD}$=5V | | 2.3 | | |
| | | | $V_{DD}$=4.2V | | 1.6 | | |
| | | | $V_{DD}$=3.7V | | 1.3 | | |
| | | f=1kHz, $R_L$=8Ω, THD=10% | $V_{DD}$=5V | | 1.72 | | |
| | | | $V_{DD}$=4.2V | | 1.2 | | |
| | | | $V_{DD}$=3.7V | | 0.93 | | |
| | | f=1kHz, $R_L$=8Ω, THD=1% | $V_{DD}$=5V | | 1.39 | | |
| | | | $V_{DD}$=4.2V | | 0.97 | | |
| | | | $V_{DD}$=3.7V | | 0.75 | | |
| THD+N | Total harmonic distortion plus noise | $V_{DD}$=5V, Po=1.8W, $R_L$=4Ω | | | 0.4 | | % |
| | | $V_{DD}$=5V, Po=1W, $R_L$=8Ω | | | 0.3 | | |
| PSRR | Supply ripple rejection ratio | $V_{DD}$=5V, inputs ac-grounded with $C_i$= 2uF, V(ripple)=200mV | f=217Hz | | -60 | | dB |
| | | | f=1kHz | | -62 | | dB |
| $V_n$ | Output noise voltage | Inputs ac-grounded with Ci=0.47μF, $V_{DD}$=5V | | | 35 | | uV |
| SNR | Signal-to-noise ratio | $V_{DD}$=5V, f=1kHz, THD=1% | | | 98 | | dB |
| $V_{SD\_H}$ | Shutdown Voltage Input High | $V_{DD}$=2.5V to 5.5V | | 1.4 | | | V |
| $V_{SD\_L}$ | Shutdown Voltage Input Low | $V_{DD}$=2.5V to 5.5V | | | | 0.4 | V |
| $T_{WU}$ | Wake-up time | | | | 150 | | ms |

## Typical Performance Characteristics

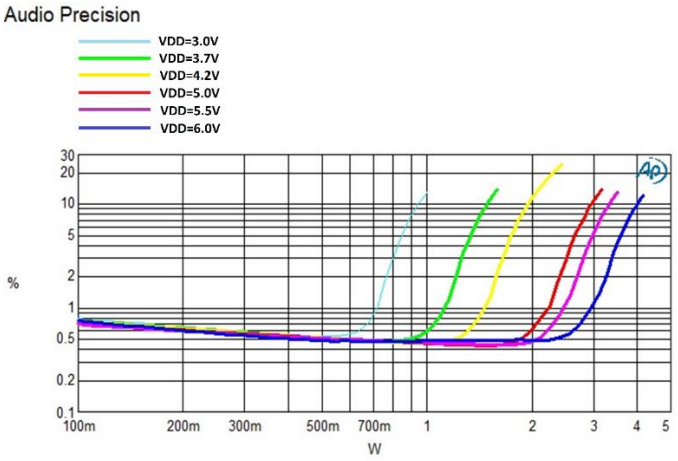



Figure 3. $P_o$ VS THD, $R_L$=4Ω

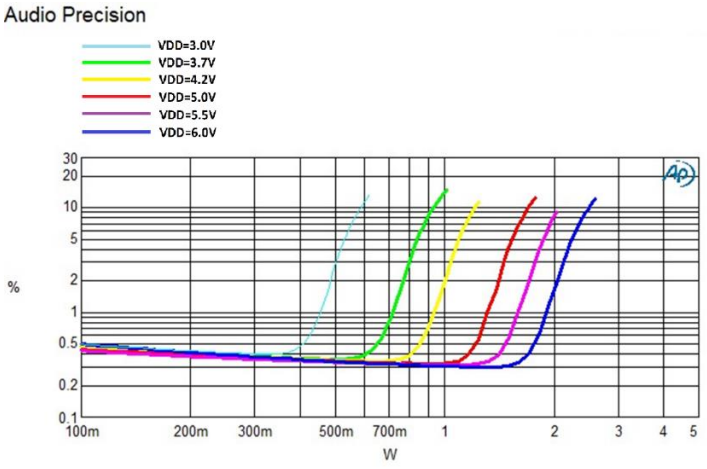
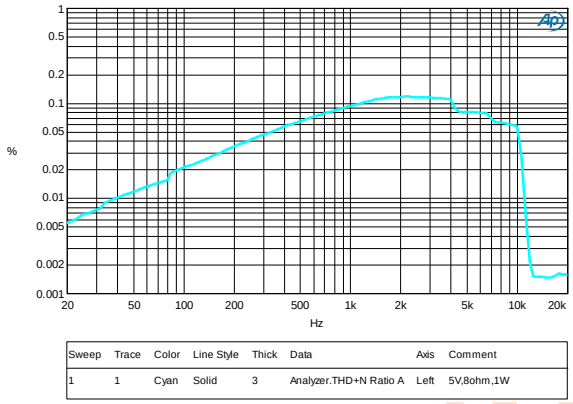



Figure 4. $P_o$ VS THD, $R_L$=8Ω




| Sweep | Trace | Color | Line Style | Thick | Data | Axis | Comment |
|---|---|---|---|---|---|---|---|
| 1 | 1 | Cyan | Solid | 3 | Analyzer.THD+N Ratio A | Left | 5V,8ohm,1W |

Figure 5. THD+N at VDD=5V, $P_o$ =1W, $R_L$=8Ω

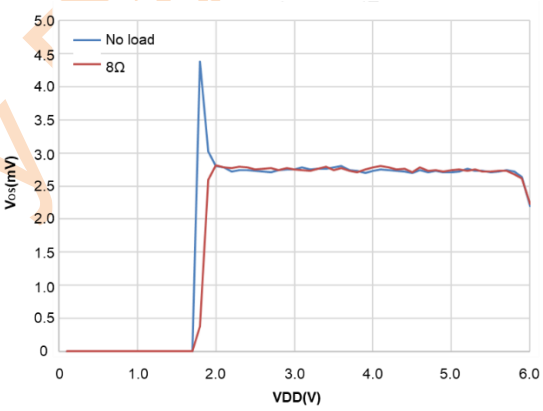



Figure 6. $V_{OS}$(VO1-VO2)

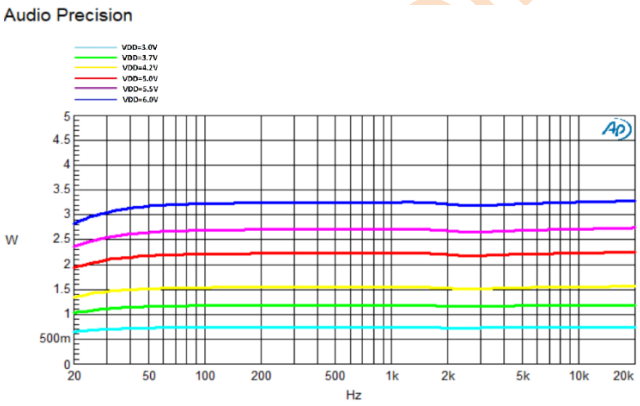



Figure 7. $P_O$ VS Freq, THD+N =1%, $R_L$=4Ω

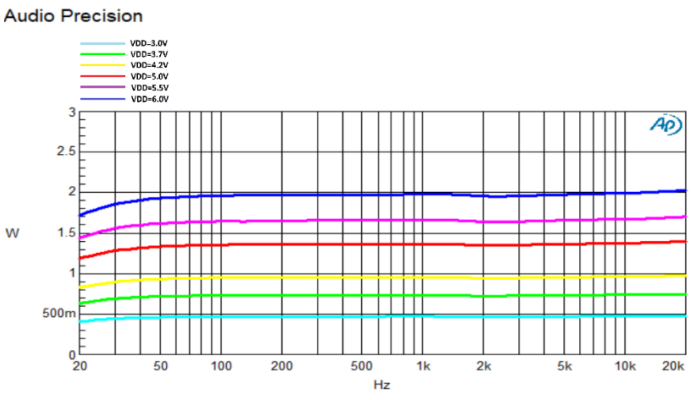



Figure 8. $P_O$ VS Freq, THD+N =1%, $R_L$=8Ω

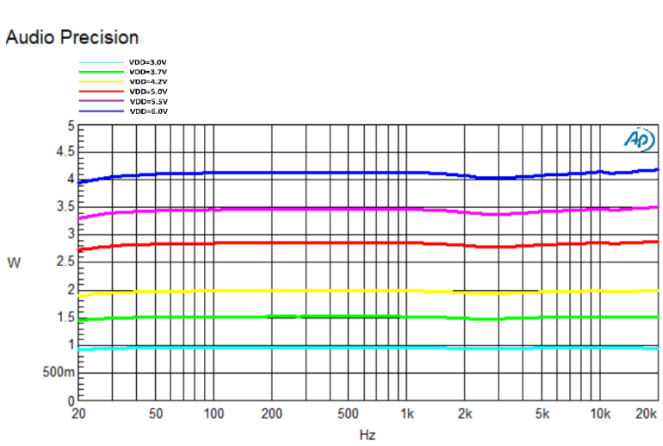



Figure 9. $P_O$ VS Freq, THD+N =10%, $R_L$=4Ω

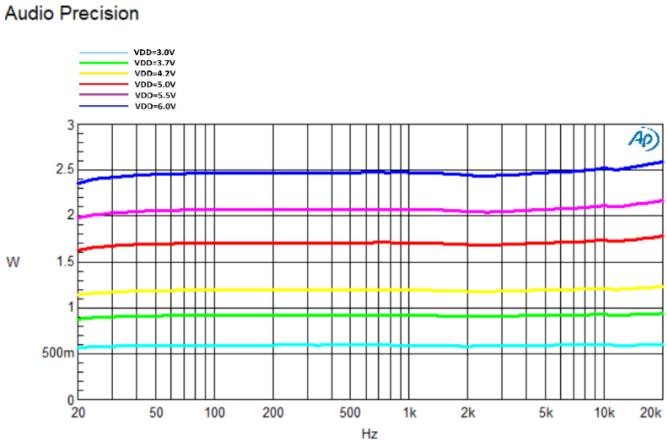



Figure 10. $P_O$ VS Freq, THD+N =10%, $R_L$=8Ω

# Function Description

## General Description

As shown in Figure 2, the LPA4871 has two operational amplifiers internally, allowing for a few different amplifier configurations. The first amplifier's gain is externally configurable, while the second amplifier is internally fixed in a unity-gain, inverting configuration. The closed-loop gain of the first amplifier is set by selecting the ratio of $R_F$ to $R_{IN}$ while the second amplifier's gain is fixed by the two internal 20kΩ resistors. Figure 2 shows the output of the amplifier one serves as the input to amplifier two, which results in both amplifiers producing signals identical in magnitude, but out of phase by 180°. Consequently, the differential gain for the IC is

$$A_{VD} = 2 \times \frac{R_F}{R_{IN}}$$

By driving the load differentially through outputs VO1 and VO2, an amplifier configuration commonly referred to as “BTL mode” is established. BTL mode operation is different from the classical single-ended amplifier configuration where one side of the load is connected to ground.

A BTL amplifier design has a few distinct advantages over the single-ended configuration, as it provides differential drive to the load, thus doubling output swing for a specified supply voltage. Four times the output power is possible as compared to a single-ended amplifier under the same conditions. This increase in attainable output power assumes that the amplifier is not current limited or clipped.

A BTL configuration, such as the one used in the LPA4871, also creates a second advantage over single-ended amplifiers. Since the differential outputs, VO1 and VO2, are biased at half-supply, no net DC voltage exists across the load. This eliminates the need for an output coupling capacitor, which is required in a single supply, single-ended amplifier configuration. Without an output coupling capacitor, the half-supply bias across the load would result in both increased internal IC power dissipation and also possible loudspeaker damage.

## Power Supply Bypassing

As with any amplifier, proper supply bypassing is critical for low noise performance and high-power supply rejection. The capacitor location on both the bypass and power supply pins should be as close to the device as possible. Typical applications employ a 5V regulator with 10 µF tantalum or electrolytic capacitor and a ceramic bypass capacitor that aid in supply stability. This does not eliminate the need for bypassing the supply nodes of the LPA4871. The selection of a bypass capacitor, especially $C_{BYP}$, is dependent upon PSRR requirements, click and pop performance, system cost, and size constraints.

## Shutdown Function

In order to reduce power consumption while not in use, the LPA4871 contains a shutdown pin to externally turn off the amplifier's bias circuitry. This shutdown feature turns the amplifier off when a logic high is placed on the SHDN pin. The LPA4871 has an internal pull-up resistor on the SHDN pin, if SHDN pin is floating, then the device will shut down. By switching the SHDN pin to logic high or pull it up to VDD, the LPA4871 supply current draw will be minimized to shutdown current($I_{SHDN}$), which is 0.1uA in typical.

In many applications, a microcontroller or microprocessor output is used to control the shutdown circuitry to provide a quick, smooth transition into shutdown. Another solution is to use a single-pole, single-throw switch in conjunction with an external pull-up resistor, refer to Figure 2. When the switch is closed, the SHDN pin is connected to ground and turn-on the amplifier. If the switch is open, then the internal pull-up resistor will disable the LPA4871. This scheme ensures that the SHDN pin will not float thus preventing unwanted state changes.

## Thermal Shutdown

The LPA4871 has thermal shutdown protection to fully protect the device from internally or externally generated excessive temperatures. The thermal shutdown circuit is activated when the die temperature exceeds a safe temperature (typ 170°C) and the switch is turned off. The switch automatically turns on again if the temperature drops below the threshold temperature.

# Application Information

## Capacitor Consideration

External capacitor on VDD is recommended in application,1μF for $C_{VDD}$ at least. Closer placement of the capacitors to the device would be better for stability.

## Power Dissipation

Power dissipation is a major concern when designing a successful amplifier, whether the amplifier is bridged or single-ended. A direct consequence of the increased power delivered to the load by a bridge amplifier is an increase in internal power dissipation. Since the LPA4871 has two operational amplifiers in one package, the maximum internal power dissipation is 4 times of a single-ended amplifier. The maximum power dissipation for a given application can be derived from the power dissipation graphs or from below Equation.

$$P_D = 4 * V_{DD}^2 / (2\pi^2 R_L)$$

$P_D$: Power Dissipation (W)

$V_{DD}$: Input voltage (V)

$R_L$: Speaker resistance (Ω)

$$T_J = P_D \times \theta_{JA} + T_A$$

$T_J$: Junction temperature (°C)

$\theta_{JA}$: Package thermal resistance (°C /W) (Note 3)

$T_A$: Ambient temperature (°C)

It is critical that the maximum junction temperature $T_{JMAX}$ of 150°C is not exceeded. $T_{JMAX}$ can be determined from the power derating curves by using $P_{DMAX}$ and the PC board foil area. By adding additional copper foil, the thermal resistance of the application can be reduced, resulting in higher $P_D$. Additional copper foil can be added to any of the leads connected to the LPA4871. If $T_{JMAX}$ still exceeds 150°C, then additional changes must be made. These changes can include reduced supply voltage, higher load impedance, or reduced ambient temperature. Internal power dissipation is a function of output power. Refer to the Typical Performance Characteristics curves for power dissipation information for different output powers and output loading.

***Note 3: The calculation base on thermal resistance is only valid in Lab condition. The value of $\theta_{JA}$ could change in customer PCB environment.**

## PCB Layout Guidelines

As output power increases, interconnect resistance (PCB traces and wires) between the amplifier, load and power supply creates a voltage drop. The voltage loss on the traces between the LPA4871 and the load results is lower output power and decreased efficiency. Higher trace resistance between the supply and the LPA4871 has the same effect as a poorly regulated supply, increase ripple on the supply line also reducing the peak output power. The effects of residual trace resistance increases as output current increases due to higher output power, decreased load impedance or both. To maintain the highest output voltage swing and corresponding peak output power, the PCB traces that connect the output pins to the load and the supply pins to the power supply should be as wide as possible to minimize trace resistance.

The use of power and ground planes will give the best THD+N performance. While reducing trace resistance, the use of power planes also creates parasite capacitors that help to filter the power supply line.

The inductive nature of the transducer load can also result in overshoot on one or both edges, clamped by the parasitic diodes to GND and VDD in each case. From an EMI stand- point, this is an aggressive waveform that can radiate or conduct to other components in the system and cause interference. It is essential to keep the power and output traces short and well shielded if possible. Use of ground planes, beads, and micro-strip layout techniques are all useful in preventing unwanted interference.

As the distance from the LPA4871 and the speaker increase, the amount of EMI radiation will increase since the output wires or traces acting as antenna become more efficient with length. What is acceptable EMI is highly application

specific.

Ferrite chip inductors placed close to the LPA4871 may be needed to reduce EMI radiation. The value of the ferrite chip is very application specific.

Some general mixed signal layout recommendations as below:

**1. Power and Ground Circuits**

For 2-layer mixed signal design, it is important to isolate the digital power and ground trace paths from the analog power and ground trace paths. Star trace routing techniques (bringing individual traces back to a central point rather than daisy chaining traces together in a serial manner) can have a major impact on low level signal performance. Star trace routing refers to using individual traces to feed power and ground to each circuit or even device. This technique will require a greater amount of design time but will not increase the final price of the board. The only extra parts required will be some jumpers.

**2. Single-Point Power / Ground Connections**

The analog power traces should be connected to the digital traces through a single point (link). A "Pi-filter" can be helpful in minimizing High Frequency noise coupling between the analog and digital sections. It is further recommended to put digital and analog power traces over the corresponding digital and analog ground traces to minimize noise coupling.

**3. Placement of Digital and Analog Components**

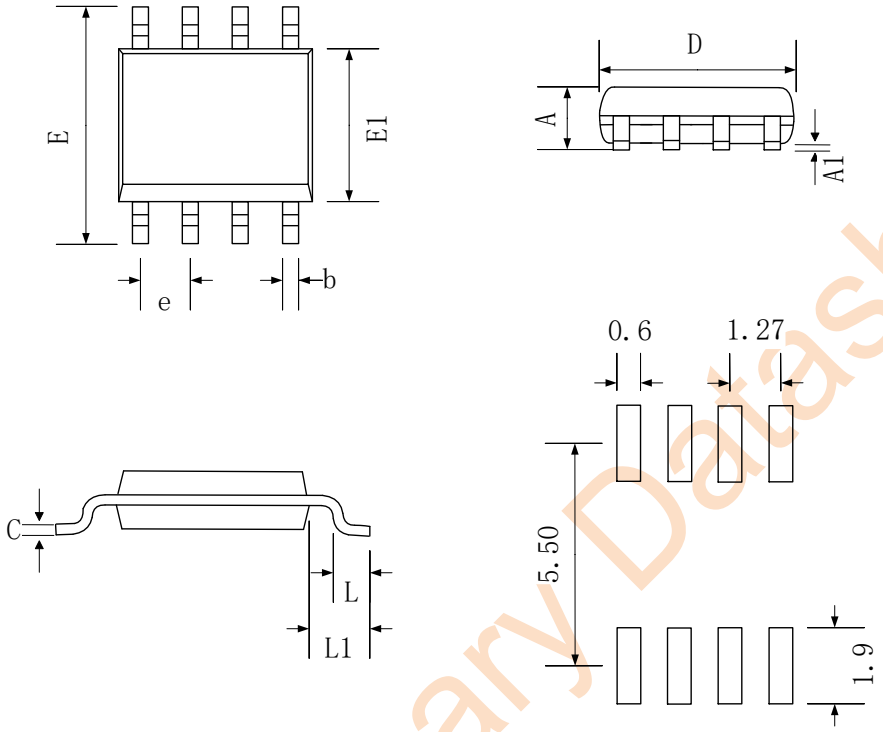
All digital components and high-speed digital signals traces should be located as far away as possible from analog components and circuit traces.

**4. Avoiding Typical Design / Layout Problems**

Avoid ground loops or running digital and analog traces parallel to each other (side-by-side) on the same PCB layer. When traces must cross over each other do it at 90 degrees. Running digital and analog traces at 90 degrees to each other from the top to the bottom side as much as possible will minimize capacitive noise coupling and cross talk.

## Package Information

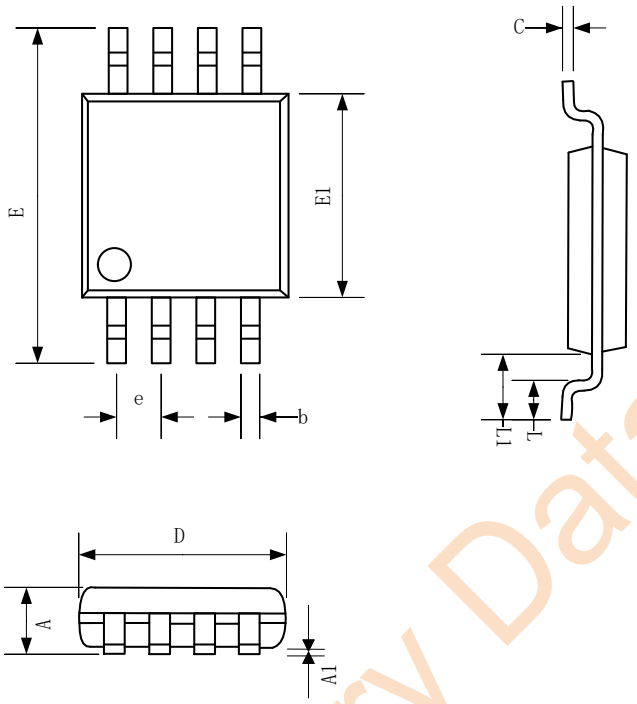
### SOP-8




Recommended Land Pattern

| SYMBOL | Dimensions In Millimeters | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | 1.35 | - | 1.75 |
| A1 | 0.10 | - | 0.25 |
| b | 0.30 | 0.40 | 0.50 |
| c | | 0.20 REF | |
| D | 4.70 | 4.90 | 5.10 |
| E | 5.70 | 6.00 | 6.30 |
| E1 | 3.70 | 3.90 | 4.10 |
| e | | 1.27 BSC | |
| L | 0.40 | 0.60 | 0.80 |
| L1 | | 1.05 REF | |

## MSOP-8




| SYMBOL | Dimensions In Millimeters | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | - | - | 1.10 |
| A1 | 0.00 | - | 0.15 |
| b | 0.22 | 0.30 | 0.38 |
| c | | 0.17REF | |
| D | 2.90 | 3.00 | 3.10 |
| E | 4.70 | 4.90 | 5.10 |
| E1 | 2.90 | 3.00 | 3.10 |
| e | | 0.65BSC | |
| L | 0.40 | 0.60 | 0.80 |
| L1 | | 0.95 REF | |