

Features

- Wide input voltage range: 4.2V – 16V
- Output voltage range: $V_{ref} - 7V$
- High efficiency operation
 - Integrated an 75-mΩ LS-MOSFET and an 110-mΩ HS-MOSFET
 - 92% efficiency at 2A load from 12V to 5V conversion
- Automatic PFM mode at light load
- $\pm 1\%$ Vref accuracy
- Typical 1.2-MHz switching frequency
- COT control scheme with fast load transient response
- Hiccup protection
- Integrated UVLO, OVP, OCP, SCP, and OTP protections
- 0.8ms typical soft-start time
- 1.6mm X 2.9mm SOT23-6 package
- RoHS Compliant and 100% Lead (Pb) Free
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Applications

- Industrial PC
- Network/digital video recorder (NVR/DVR)
- TV and TV box
- 12V Industrial bus applications

General Description

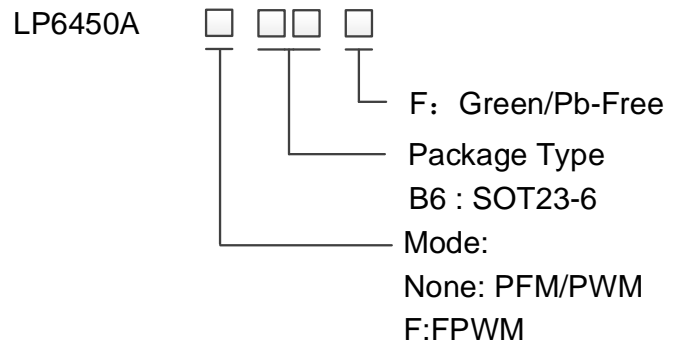
The LP6450A is a synchronous buck converter supporting up to 2A output current. The LP6450A employs an adaptive constant-on-time (COT) control scheme to achieve fast load transient response. The external components are minimized, requiring only one inductor, two resistors, and two capacitors.

The LP6450A supports both aluminum polymer capacitors and ceramic capacitors without extra compensation components.

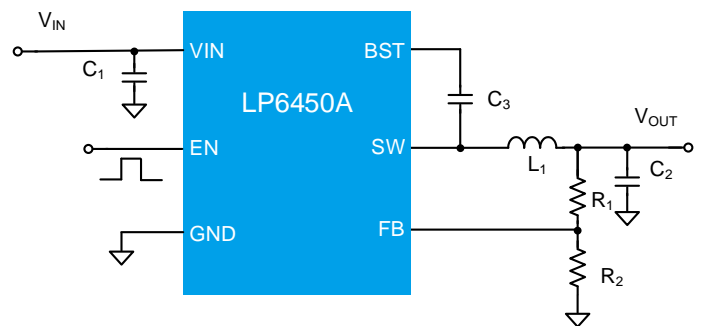
The LP6450A integrates PFM (Pulse Frequency Modulation) operation, which helps maintain the system efficiency at light load. The LP6450A also integrates multiple protection functions, i.e., over-current protection (OCP), over-temperature protection (OTP), under-voltage lockout (UVLO), and short circuit protection (SCP).

The LP6450A is available in a small 6-pin 1.6mmX2.9mm SOT23-6 package.

Order Information



Typical Application Circuit





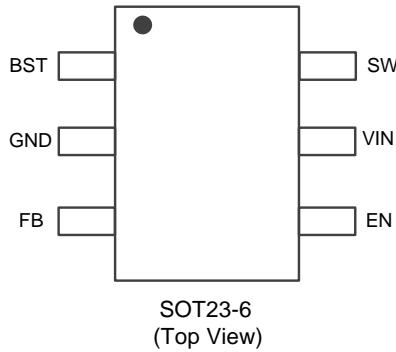
Device Information

Part Number	Top Marking	Vref	MODE	Package	Shipping
LP6450AB6F	K5 YWX	0.6V	PFM/PWM	SOT23-6	3K/REEL
LP6450AFB6F	K6 YWX	0.6V	FPWM	SOT23-6	3K/REEL

Marking indication: Y: Year code. W: Week code. X: Batch numbers.



Pin Diagram



Pin Description

Pin #	Name	Description
1	BST	Bootstrap pin. Power supply for high-side MOSFET gate driver. A 0.1- μ F capacitor must be connected between this pin and SW pin.
2	GND	Power ground of the IC
3	FB	Feedback pin. Use a resistor divider to set the desired output voltage
4	EN	Enable input. This pin can be used to control the system power sequence as well
5	VIN	IC power supply input.
6	SW	The switching node of the converter.



Absolute Maximum Ratings (Note)

VIN, SW, and EN to GND	-----	-0.3V to 18V
FB to GND	-----	-0.3V to 6.5V
BST to SW	-----	-0.3V to 6.5V
SW to GND (20ns transient)	-----	-3.5V to 20V
Junction Temperature Range (T _J)	-----	-40°C to 150°C
Maximum Soldering Temperature (at leads, 10 sec)	-----	-260°C

Note: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD Ratings

HBM (Human Body Model)	-----	2kV
CDM (Charged-device Model)	-----	500V

Thermal Information

θ _{JA} (Junction-to-Ambient Thermal Resistance)	-----	160°C/W
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Recommended Operating Conditions

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V _{IN}	Input voltage	4.2		16	V
V _{OUT}	Output voltage	V _{ref}		7	V
L	Inductor	0.7		6.0	μH
T _A	Ambient temperature range	-40		105	°C
C _{IN}	Input decoupling capacitor	4.7		100	μF
C _{OUT}	Output capacitor	10		100	μF

Electrical Characteristics

(The specifications are measured under conditions V_{IN} = 12V, T_J = 25°C, unless otherwise specified.)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SECTION						
V _{ULVO_R}	Input voltage under lockout threshold	V _{IN} rising threshold		3.8	4.2	V
V _{ULVO_H}	UVLO hysteresis	V _{IN} falling threshold		0.15		V
V _{OVP_R}	Input over voltage protection threshold	V _{IN} rising threshold		16.1		V
V _{OVP_F}	OVP hysteresis	V _{IN} falling threshold		0.5		V
I _{q_VIN}	Input quiescent current	No switching, EN=3V, FB=1.0V		300		μA



SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I _{SD}	Shutdown current	EN=0		1.5		μA
BUCK CONVERTER						
I _{LIM}	Low-side valley current limit	T _J =25°C	2.2	3.2	4.2	A
V _{ref}	Reference voltage	T _J =25°C,	0.584	0.592	0.6	V
		-40~125 °C,	0.574		0.61	V
R _{dson_HS}	High-side FET on resistance	V _{IN} =12V		110		mΩ
R _{dson_LS}	Low-side FET on resistance	V _{IN} =12V		75		mΩ
F _{sw}	Switching frequency			1200		kHz
t _{on-min}	Minimum on-time ^[1]			50		ns
t _{off-min}	Minimum off-time ^[1]	V _{FB} =V _{ref} - 0.2V		100		ns
t _{on-hiccup}	Hiccup on time ^[1]	Including soft start time		1.5		ms
t _{off-hiccup}	Hiccup waiting time ^[1]			25		ms
t _d	EN delay time ^[1]	From EN high to first switching		150		us
t _{ss}	Soft-start time ^[1]	From first switching to 95%V _{ref}		860		us
T _{jsd}	Thermal shutdown threshold	Rising threshold		160		°C
	Thermal shutdown threshold	Falling threshold		135		°C
I _{leak_FB}	FB pin leakage current			0.01		μA
EN Logic						
V _H	EN pin logic high threshold	EN Rising threshold		1.2		V
V _{hys}	EN pin threshold hysteresis			0.1		V
	EN pin internal pull-down resistance			1000		kΩ

[1]: Not production tested. Guaranteed by design



Typical Characteristics

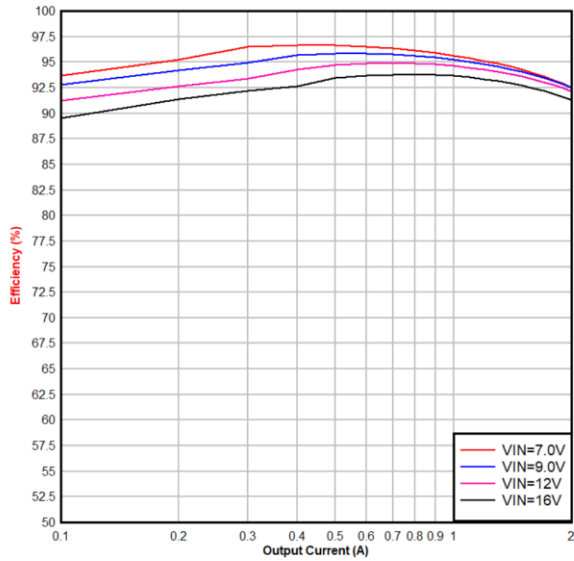


Figure 1. Vout=5V, Efficiency, L=4.7uH

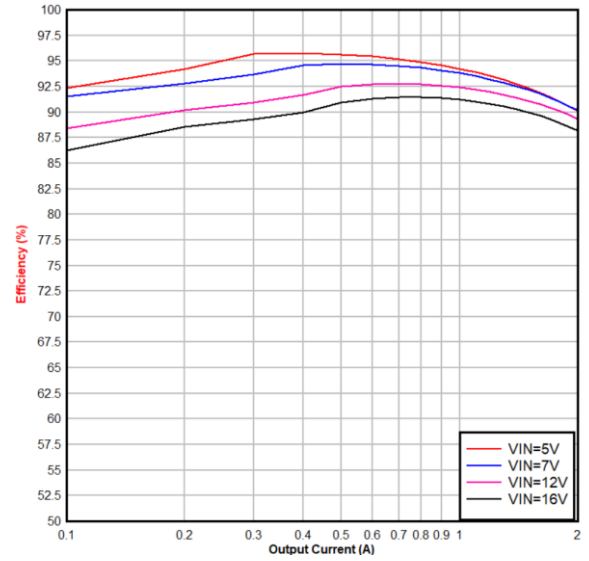


Figure 2. Vout=3.3V, Efficiency, L=3.3uH

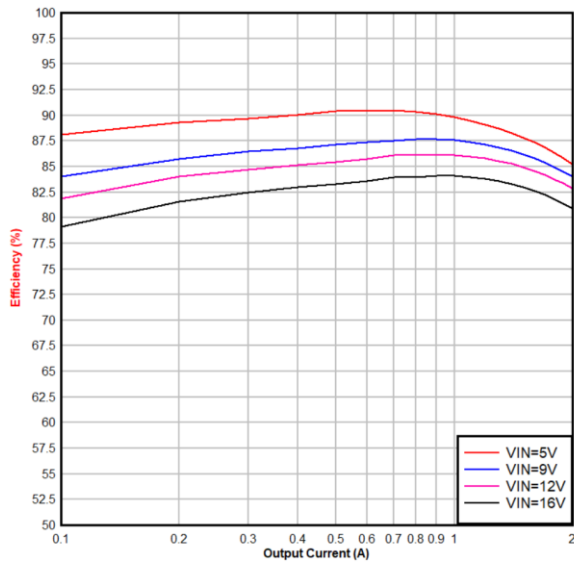


Figure 3. Vout=1.8V, Efficiency, L=1.5uH

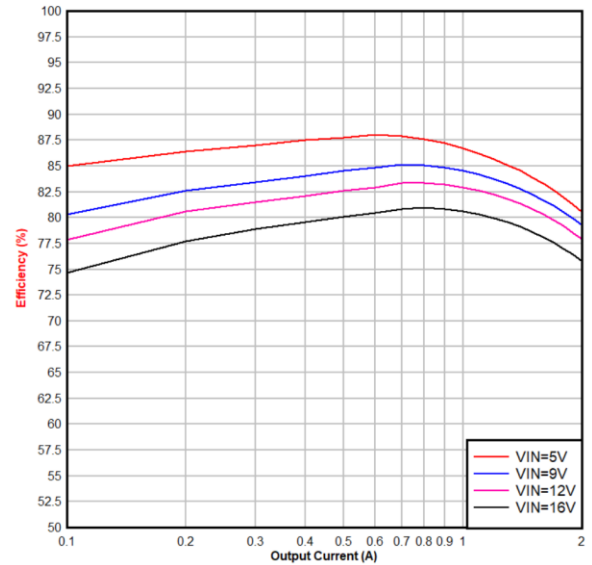


Figure 4. Vout=1.2V, Efficiency, L=1.5uH

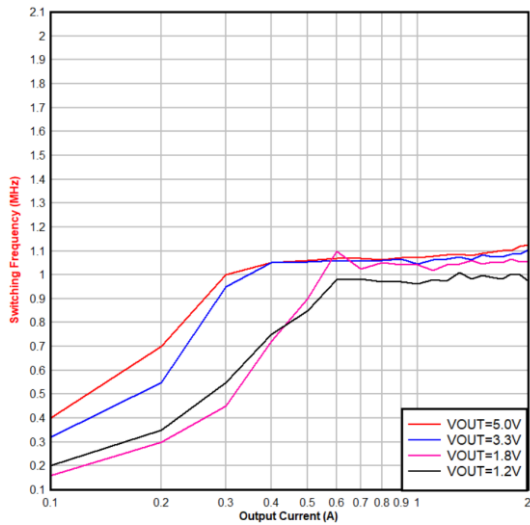


Figure 5. Switching Frequency VS. Output Current

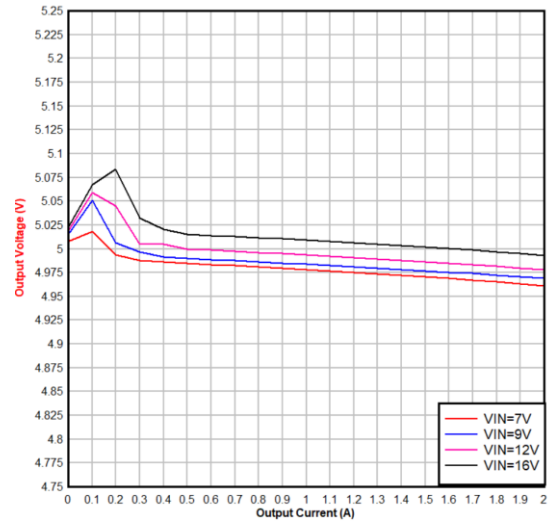


Figure 6. VOUT=5V, Regulation, L=4.7uH

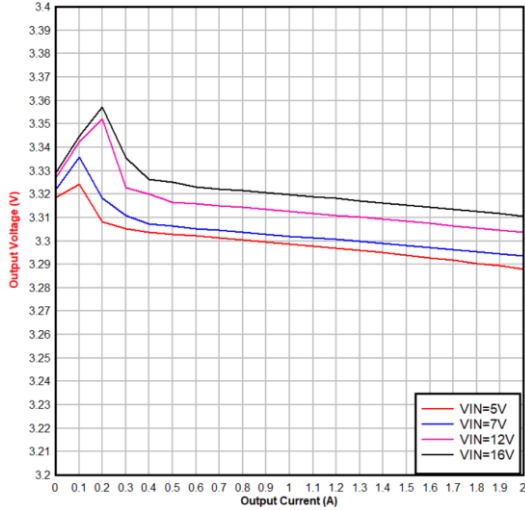


Figure 7. VOUT=3.3V, Regulation, L=3.3uH

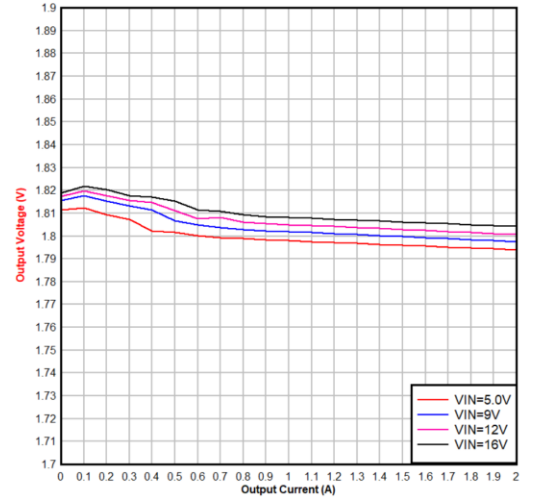


Figure 8. VOUT=1.8V, Regulation, L=1.5uH

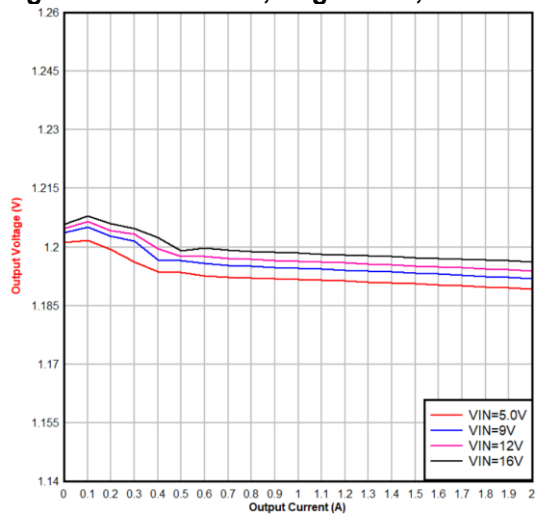


Figure 9. VOUT=1.2V, Regulation, L=1.5uH



Application Waveforms (Vin=12V, L=4.7uH, Cout=22uF*2)

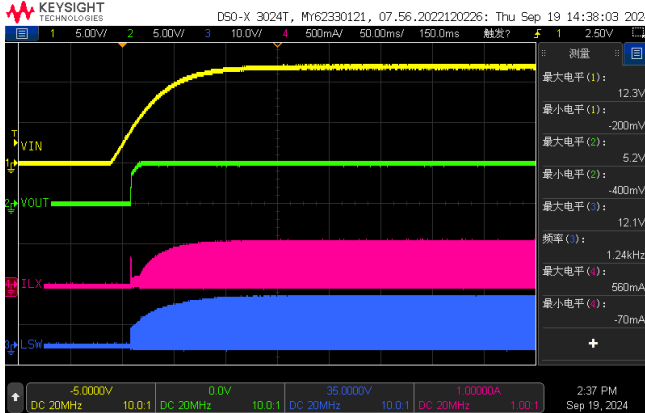


Figure 10. Startup by VIN, 100Ω load

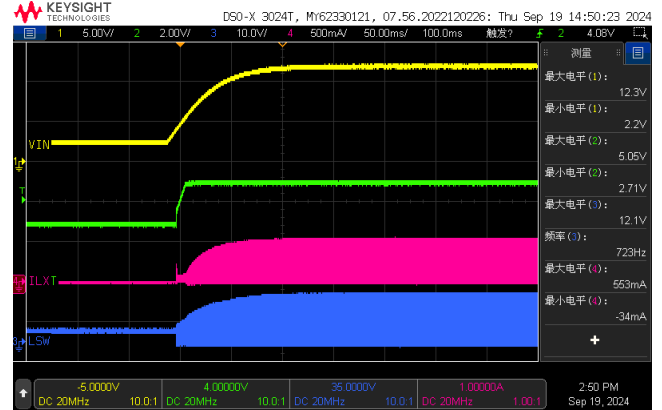


Figure 11. Prebias Startup by VIN, 100Ω load

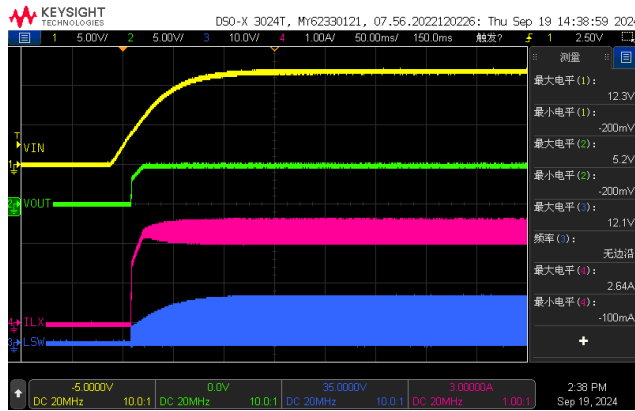


Figure 12. Startup by VIN, 2Ω load

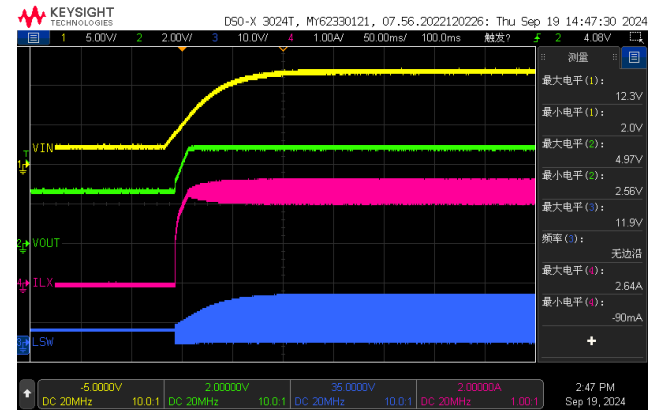


Figure 13. Prebias Startup by VIN, 2Ω load

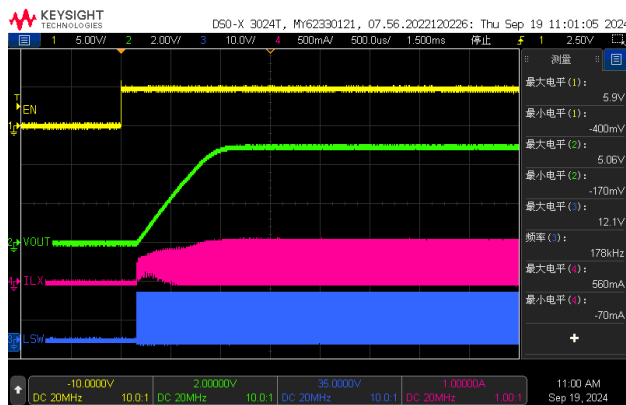


Figure 14. Startup by EN, 100Ω load

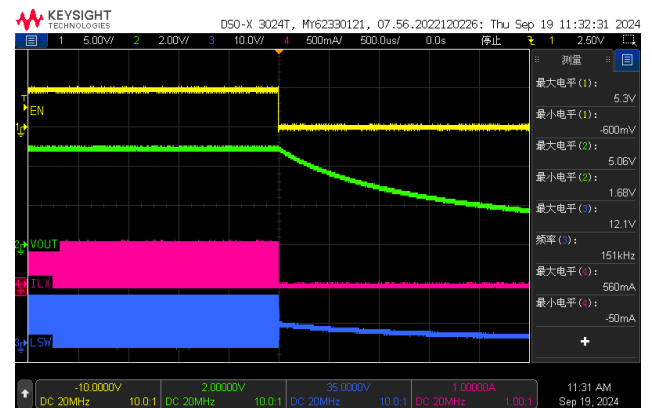


Figure 15. Shutdown by EN, 100Ω load

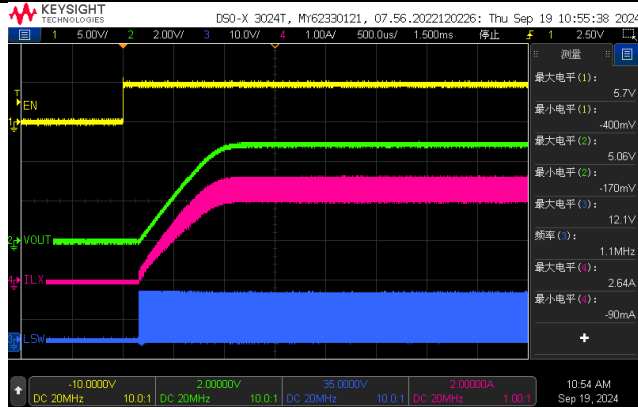


Figure 16. Startup by EN, 2Ω load

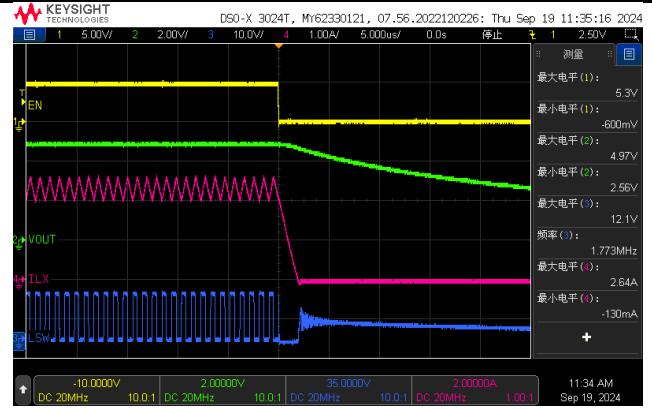


Figure 17. Shutdown by EN, 2Ω load

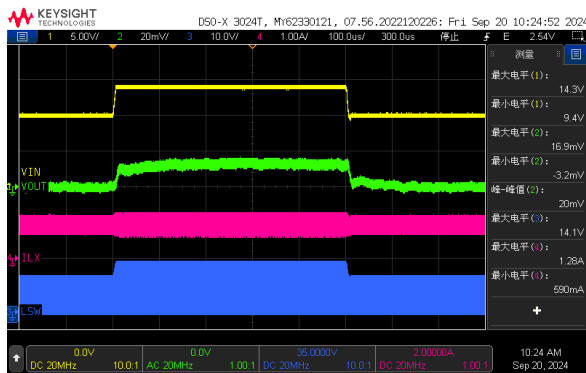


Figure 18. Line Transient, 1A load

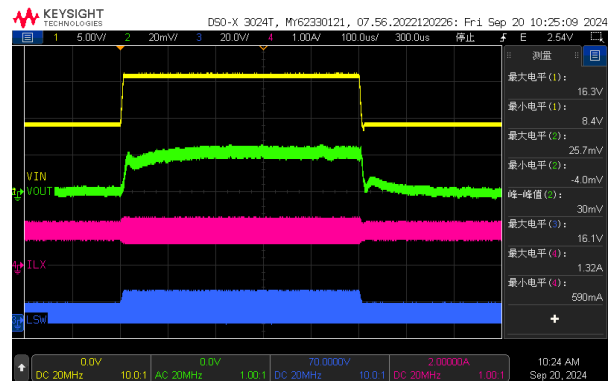


Figure 19. Line Transient, 1A load

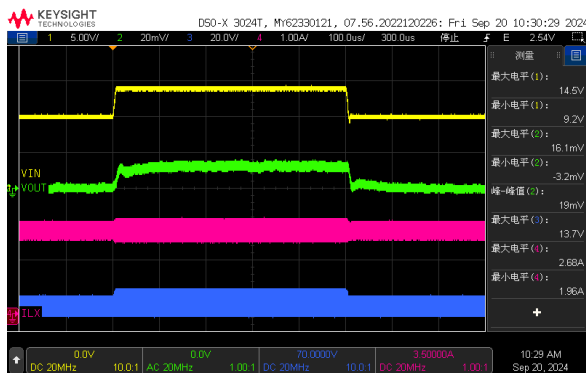


Figure 20. Switching Waveform, 2A load

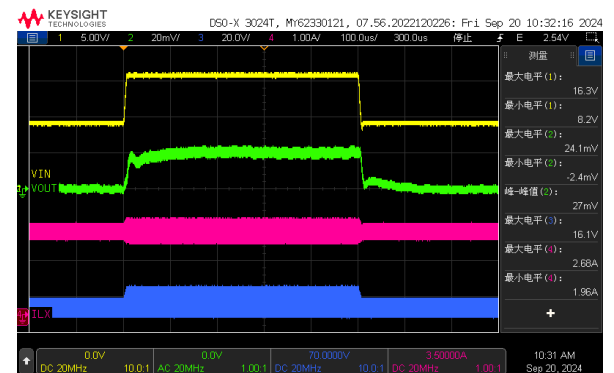


Figure 21. Line Transient, 2A load

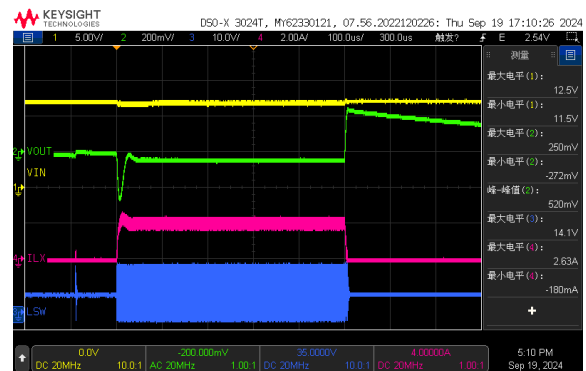


Figure 22. Load Transient, 0A-2A-0A

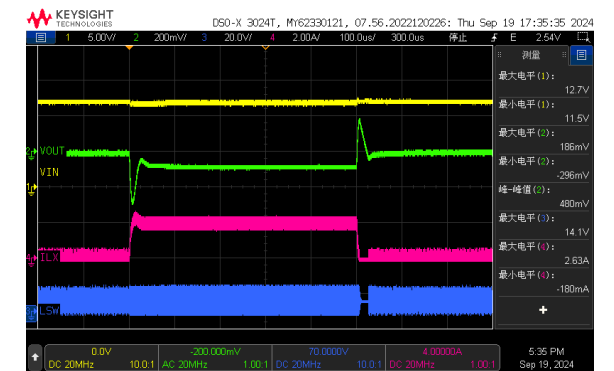


Figure 23. Load Transient, 0.1A-2A-0.1A

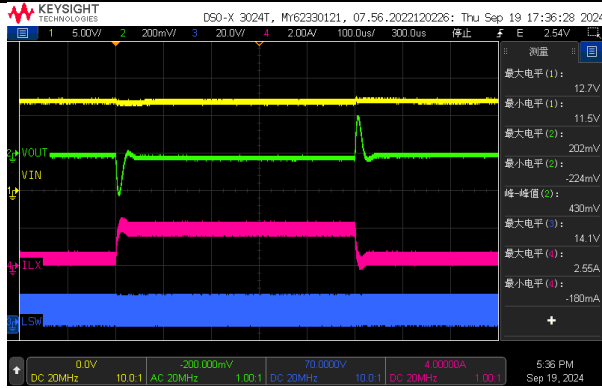


Figure 24. Load Transient, 0.5A-2A-0.5A

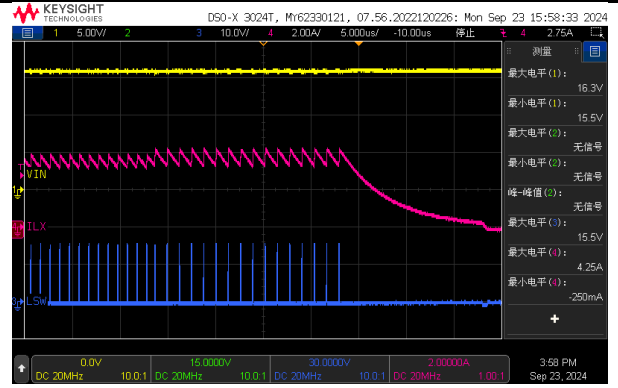


Figure 25. Current Limit Operation

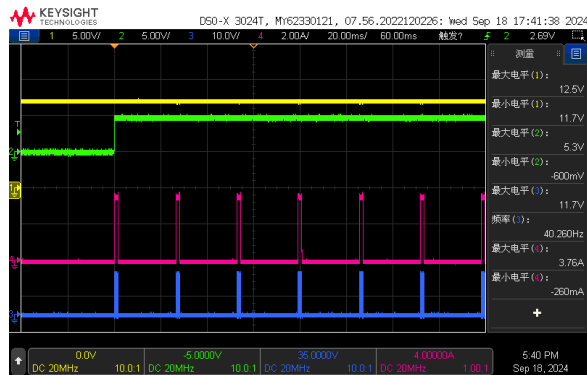
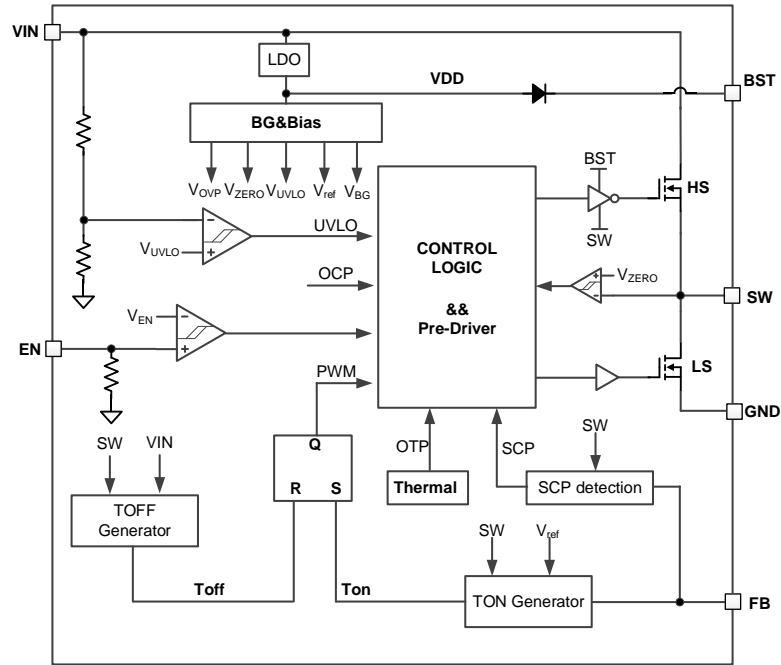


Figure 26. Short Circuit Startup and Hiccup Protection



Functional Block Diagram





Detailed Description

Overview

The LP6450A is a 2A synchronous buck converter, supporting 4.2-16V input voltage range. The adaptive COT control scheme enables fast transient respond and minimizes the output capacitance. The LP6450A supports both aluminum polymer capacitors and low-ESR ceramic capacitors without external compensation circuit. The LP6450A automatically transfers between PFM and PWM according to the output current.

Under Voltage Lockout (UVLO)

When the input voltage V_{IN} is lower than the UVLO threshold, all functions are shut down. When the input voltage is higher than the UVLO rising threshold, the LP6450A can be enabled by the EN pin.

EN Control

The EN pin can be used to control the system power-up sequence. A precise voltage reference is used as the threshold. When the V_{IN} is above the UVLO threshold and EN voltage rises above the EN pin logic high threshold (1.2V typically), the LP6450A enables all the internal circuits, delays for 260us, and begins the soft-start (refer to Soft-start section for more details).

The EN pin has an internal 1000k Ω pull-down resistor to ground.

Soft-start

The LP6450A integrates soft-start function with a typical time of 0.8ms (t_{ss}). After passing the UVLO threshold and enabled by the EN pin with the 150us delay(t_d), the internal reference voltage ramps from zero to the V_{ref} in 0.8-ms and the output voltage ramps up accordingly.

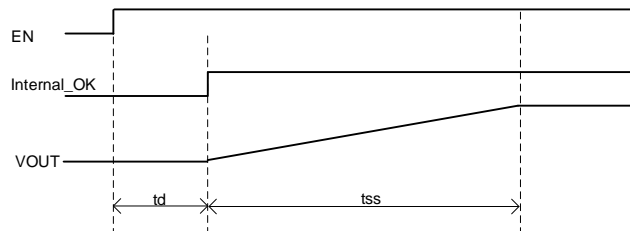


Figure 27. Soft Start Sequence

Constant-ON Time (COT) Control Scheme

The LP6450A integrates the COT control scheme for pseudo-fixed- frequency operation when operating in continuous conduction mode (CCM). Refer to the Functional Block Diagram for better understanding of the operation. The internal on-time (TON) generator block monitors the FB-pin voltage and turns on the high-side MOSFET to start a switching cycle, when the FB-pin voltage drops to an internal reference voltage V_{ref} . Then the internal circuits start to calculate the on-time of the high-side MOSFET, which is proportional to the input voltage and inversely proportional to the output voltage. Once the on-time is finished, the TOFF generator turns off the high-side MOSFET and turns on the low-side MOSFET.

PFM Operation

The LP6450A is designed to maintain high efficiency at light load by adopting pulse-frequency modulation (PFM). In the PFM, the switching cycle is still initiated by the TON generator monitoring the FB-pin voltage. The high-side MOSFET is turned on for TON time and then turned off, followed by turning on the low-side MOSFET. The inductor current falls when the low-side MOSFET is on. When the inductor current reaches zero, detected by the zero-current detection (ZCD) comparator, the low-side MOSFET is turned off, together with the high-side MOSFET. Both MOSFETs remains off until a new switching cycle begins, determined by TON generator. As the load current decreases, the duration for both MOSFETs to remain off increases, leading to a lower switching frequency and higher power efficiency.



Bootstrap Capacitor

The LP6450A integrates two N-MOSFET to achieve high efficiency. The high-side MOSFET is powered by the bootstrap capacitor CBST, which is between the BST pin and SW pin.

Over Current Protection and Short Circuit Protection

The LP6450A protects an over current situation by limiting the inductor valley current. The current of low-side MOSFET is monitored all the time to sense the inductor valley current when the LP6450A is enabled. The high-side MOSFET cannot be turned on if the valley current is higher than the low-side valley current limit, protecting the inductor current from further increasing. The inductor current is limited to the valley current limit plus a half of the inductor ripple current.

The SCP is realized by monitoring the FB-pin voltage when the inductor current is limited. Once the output load draws more current than the current limit, the output voltage drops. When the FB voltage drops to 50% of the Vref for 1.5-ms, the LP6450A shuts down. The LP6450A will restart after a typical 32-ms hiccup waiting time. If the SCP condition still holds after soft-start, the LP6450A shutdown again, repeating the hiccup operation.

When the over current condition is removed, the output voltage returns to normal operation.

Thermal Protection

The LP6450A has a thermal protection function. The device will shut down when the internal temperature is higher than 160°C and will restart after the temperature drops below 135°C.



Application Information

Design Requirements

The table 1 shows the design parameters for a typical 5V output voltage in the IPC application.

Table 1 Design Parameters

Parameter	Target
Input voltage range	9~15V
Output voltage	5V
Transient ripple	±200mV
Operating frequency	1200kHz

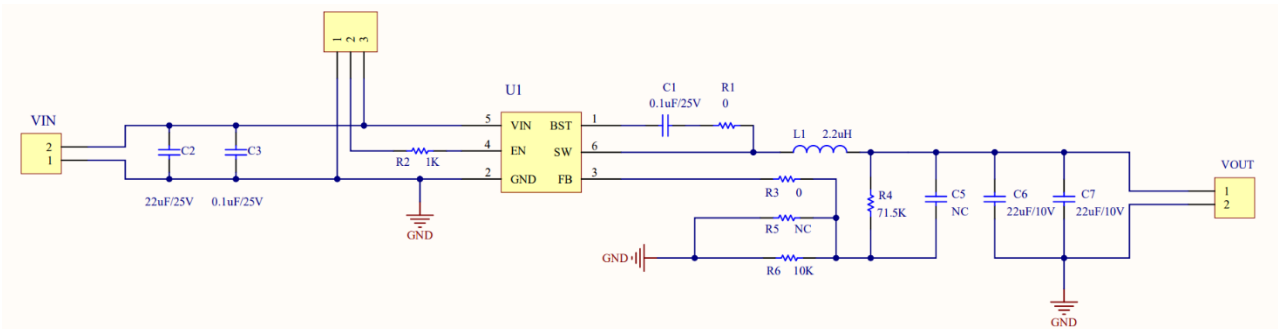


Figure 28. Typical schematic

Output Voltage Setting

The output voltage can be programmed by adjusting the external resistor divider R_{UP} and R_{DOWN} according to the equation below:

$$V_{OUT} = \left(\frac{R_{UP}}{R_{DOWN}} + 1 \right) * V_{ref}$$

When the output voltage is in regulation, the typical voltage at FB pin is 0.6V for LP6450A.

For better accuracy, the R_{DOWN} is recommended to be lower than 100kΩ to ensure the current flowing through R_{DOWN} is at least 100 times larger than the FB pin leakage current.

For a 5V-output application, a 10kΩ R_{DOWN} is selected and the R_{UP} is 73.2kΩ. R_{option} is good to have to avoid switching noise from the ground plane under heavy load.

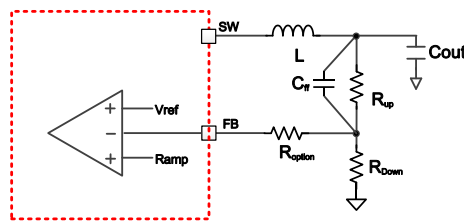


Figure 29. FB connection

EN Design

The LP6450A allows the user to design a precise VIN voltage to enable the converter during power on. The startup



sequence can be designed by adjusting the resistor divider of R_{UP_EN} and R_{DOWN_EN} with the equation below,

$$V_{EN} = \frac{1000k\Omega // R_{DOWN_EN}}{R_{UP_EN} + 1000k\Omega // R_{DOWN_EN}} * V_{IN}$$

where V_{EN} is the EN rising threshold voltage at which the converter is enabled, which is 1.2V typically. A 47pF-1nF capacitor is recommend to be soldered in parallel with the R_{EN_DOWN} to avoid the high-frequency noise influence from the switching node.

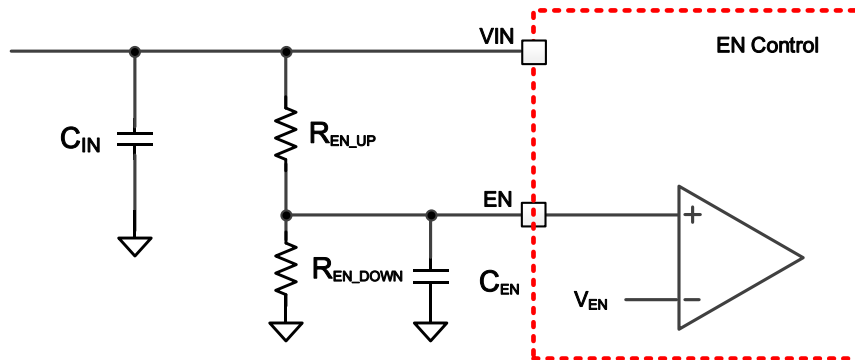


Figure 30. EN connection

Inductor and Output Capacitor Setting

The inductor ripple is calculated by the equation below:

$$I_{PP} = \left(\frac{V_{OUT}}{L * F_{SW}} * \frac{V_{IN} - V_{OUT}}{V_{IN}} \right)$$

To get a better efficiency, the inductor ripple is recommended to be controlled under 40% of the output current to minimize the AC loss of the inductor and power MOSFETs.

For a typical 12V input voltage and 5V output voltage, a low DCR value, 2.2- μ H inductor is recommended.

The output capacitor not only impacts the output ripple but also the loop stability. Please follow the design rules in the table below. A feedforward capacitor C_{FF} can be selected to improve the transient behavior. The typical capacitance can be 10-100pF. For this design, 10V, X5R, 22 μ F capacitors (GRM21BR61A226ME51) from Murata are soldered at the VOUT to GND. Multiple capacitors should be soldered to keep the system stable because of the voltage rating effect.

Table 1 Recommend R/L/C values

Vout	Inductor-L	Cout	R_{UP}	R_{DOWN}	C_{ff}
1.2V	1 μ H ~1.5 μ H	22 μ F*1	10 k Ω	10 k Ω	NA
3.3V	1.5 μ H ~3.3 μ H	22 μ F*2	45 k Ω	10 k Ω	10-100pF
5.0V	2.2 μ H ~4.7 μ H	22 μ F*3(2.2uH) 22 μ F*2(4.7uH)	73.2 k Ω	10 k Ω	10-100pF

Bootstrap capacitor

A 0.1- μ F ceramic capacitor is needed to supply power for the high-side N-MOSFET driver. The capacitor should be at least 10V.

Input capacitor

A typical 22- μ F ceramic capacitor is needed to serve as the bulk capacitor at the VIN pin. An additional 0.1 μ F is strongly recommended to provide additional high frequency filtering and should be placed to the VIN pin and GND as close as possible.



PCB Layout Guidelines

Proper layout of the components to minimize high frequency current path loop is important to prevent electrical and magnetic field radiation and high frequency resonant problems. Follow this specific order carefully to achieve the proper layout.

- Place input capacitor C_3 as close as possible to VIN pin and GND pin and use shortest copper trace connection or GND plane.
- Put output capacitor near to the inductor output terminal and the device. Ground connections need to be tied to the IC ground with a short copper trace or GND plane
- Place inductor input terminal to SW pin as close as possible and limit SW node copper area to lower electrical and magnetic field radiation. Do not use multiple layers in parallel for this connection. Minimize parasitic capacitance from this area to any other trace or plane.
- R_1 is reserved to slow down the switching speed for noise sensitive applications.

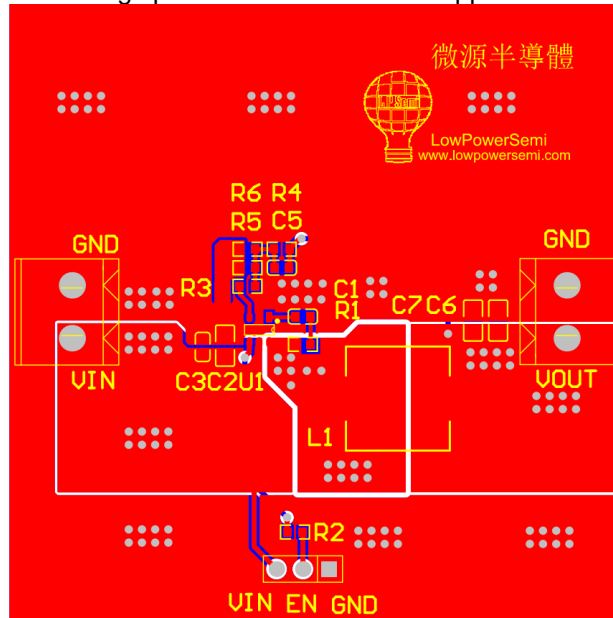
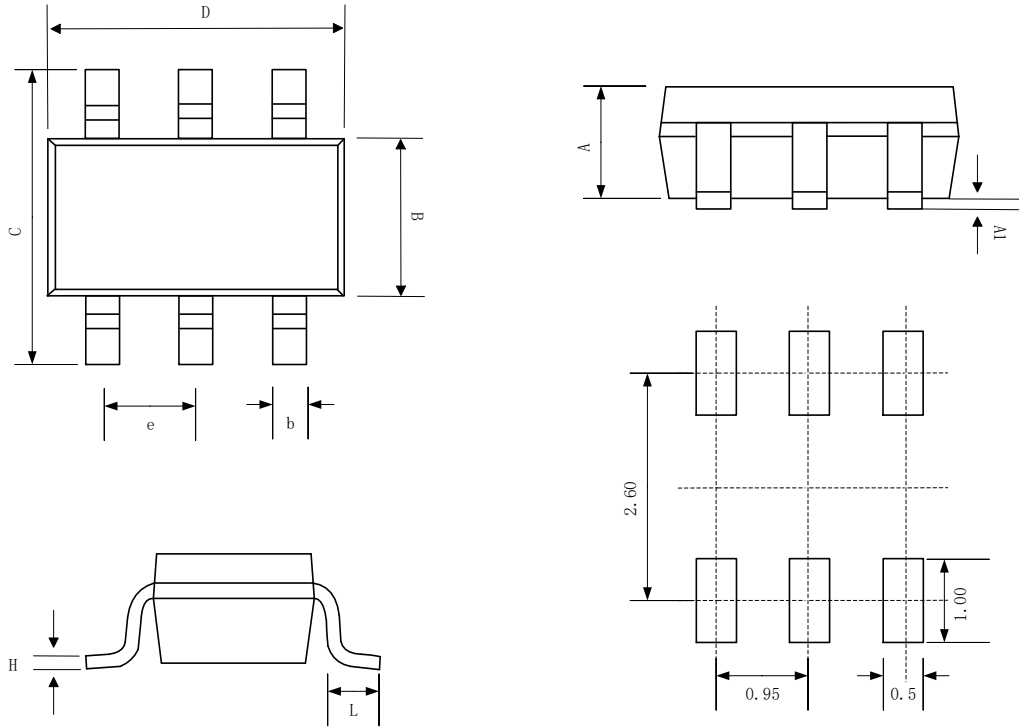


Figure 31 Layout example



Packaging Information

1.6x2.9 SOT23-6 package



Recommended Land Pattern

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.889	1.100	1.295
A1	0.000	0.050	0.152
B	1.397	1.600	1.803
b	0.28	0.35	0.559
C	2.591	2.800	3.000
D	2.692	2.920	3.120
e	0.95BSC		
H	0.080	0.152	0.254
L	0.300	0.450	0.610



Revision History

Revision	Date	Change Description
Rev 1p0	9/5/2024	First release version